RADIO FREQUENCY CIRCUITS FOR TUNABLE MULTI-BAND CMOS RECEIVERS FOR WIRELESS LAN APPLICATIONS

By

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RADIO FREQUENCY CIRCUITS FOR TUNABLE MULTI-BAND CMOS RECEIVERS FOR WIRELESS LAN APPLICATIONS

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December 2004

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Currently, three mainstream wireless LAN (WLAN) standards, IEEE 802.11a, b and g, co-exist in the market. The network should be able to work with all these standards. This has increased the demand of multi-band wireless LAN transceivers. Being a commercial application, the transceiver must be low cost, which points to a CMOS single chip solution. This dissertation addresses the design issues of multi-band CMOS WLAN receivers.

A multi-band and multi-function receiver architecture is proposed for wireless LAN applications. The key blocks include RF switches, a multi-band RF down-converter, a multi-band voltage controlled oscillator (VCO) and a wide-tuning range VCO. This thesis work demonstrates the feasibility of realizing these circuits in CMOS technology.

Two RF CMOS switches working at 2.4 GHz and 5.8 GHz were designed and tested. The 2.4-GHz switch exhibits sufficient performance for 802.11b/g applications.

The 5.8-GHz switch is the first CMOS switch to have insertion loss less than 1dB at 5.8 GHz. A way to increase the CMOS switch P_{1dB} at high frequency is also explored through two 15-GHz CMOS switch designs. Through this work, a 15-GHz CMOS switch, which has comparable insertion loss as GaAs switches is demonstrated. IP_{1dB} is 4-dB lower than that of the GaAs switch. A wide tuning range voltage controlled oscillator (VCO) has been integrated with a frequency divider to provide the second local oscillator. The demonstration of a wide tuning range VCO-divider combination with excellent phase noise is a significant step toward realizing the proposed receiver.

By using switched resonators, a dual-band down-converter which includes an LNA and a mixer has been successfully implemented in a 0.18-μm CMOS process. The down-converter incorporates band selection and gain-switching features. Compared to using two separate down-converters, this dual-band down-converter is ~40% smaller. A multi-band VCO which runs at 2.4, 2.5, 4.7 and 5 GHz has also been demonstrated. The VCO exhibits the lowest phase noise among the CMOS VCO's presented to date in all the bands. These RF blocks have sufficient performance for WLAN applications.

The successful implementations of the individual RF blocks demonstrate that it is feasible to achieve a tunable multi-band operation using a single RF block implemented in CMOS technology. A single chip multi-band CMOS WLAN receiver with reduced area is possible. Lastly, the interactions between the VCO and external interference signals which are referred as injection locking have been theoretically and experimentally investigated. Based on this, design guidelines to reduce injection locking are suggested. Understanding of this is critical for integration of a receiver with a transmitter, especially incorporating power circuits.

CHAPTER 1
INTRODUCTION

1.1 Wireless LAN Standards Brief

The wireless local area network (WLAN) market has been the fastest growing segment of the semiconductor industry in recent years. WLAN's provide a simple and flexible way for people to plug into a network. In the United States, 802.11 is a family of standards for wireless LANs, which includes 802.11a, 802.11b, 802.11g, and others. Presently, the networks using 802.11a, b and g are being widely deployed. The standards are defined by the Institute of Electrical and Electronics Engineers (IEEE).

1.1.1 IEEE 802.11b

802.11b supports 1, 2, 5.5 and 11 Mbit/s data rates at distances of 150–2000 feet without special antennas. The four modulation formats are specified by the IEEE [1], page 42: "the basic access rate shall be based on 1 Mbit/s DBPSK modulation. The enhanced access rate shall be based on 2 Mbit/s DQPSK. The higher access rates shall be based on the CCK (complementary code keying) modulation scheme for 5.5 Mbit/s and 11 Mbit/s." An optional PBCC (packet binary convolutional coding) mode is also provided for potentially enhanced performance.

The operating frequency range is 2.4–2.4835 GHz, as allocated by the regulatory bodies in USA and Europe, and is 2.471–2.497 GHz, as allocated by the regulatory authority in Japan. For high data rate channels in the USA, three channels centered at 2412, 2437 and 2462 MHz have been allocated. The channel spacing is 25 MHz and

null-to-null bandwidth is 22 MHz. The specified operating temperature range by the standard is 0 °C to 40 °C for office environment (Type I) and -30 °C to 70 °C for industrial applications (Type II).

For 11 Mbit/s CCK modulation, the receiver minimum input level sensitivity is -76 dBm measured at the antenna connector with a frame error ratio (FER) less than $8x10^{-2}$. The receiver shall also provide a maximum FER of $8x10^{-2}$ at a PSDU (physical layer convergence protocol service data unit) length of 1024 octets for a maximum input level of –10 dBm measured at the antenna. The receiver adjacent channel rejection is defined between any two channels with $\geq$25 MHz separation. The adjacent channel rejection shall be measured with an 11 Mbit/s CCK modulated input signal at -70 dBm, and a signal modulated in a similar fashion at -35 dBm in an adjacent channel as shown in Figure 1-1. Under these conditions, the FER shall be no worse than $8x10^{-2}$.

In the USA, the maximum transmit output power is 30 dBm. The transmitted spectral products shall be less than –30 dBr (dB relative to the sin(x)/x peak) for the first lobe and –50 dBr for the second lobe. The transmit spectral mask is shown in Figure 1-2. The measurements shall be made using a 100-kHz resolution bandwidth and a 100-kHz video bandwidth. The transmit modulation accuracy requirement shall be based on the difference between the actual transmitted waveform and the ideal signal waveform. Modulation

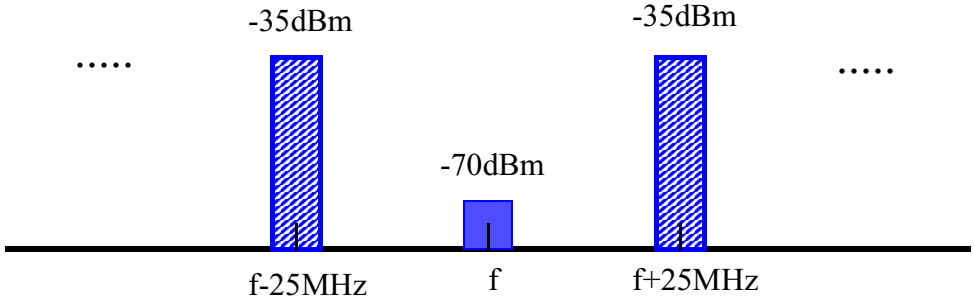


Figure 1-1 IEEE 802.11b adjacent channel rejection test input signals

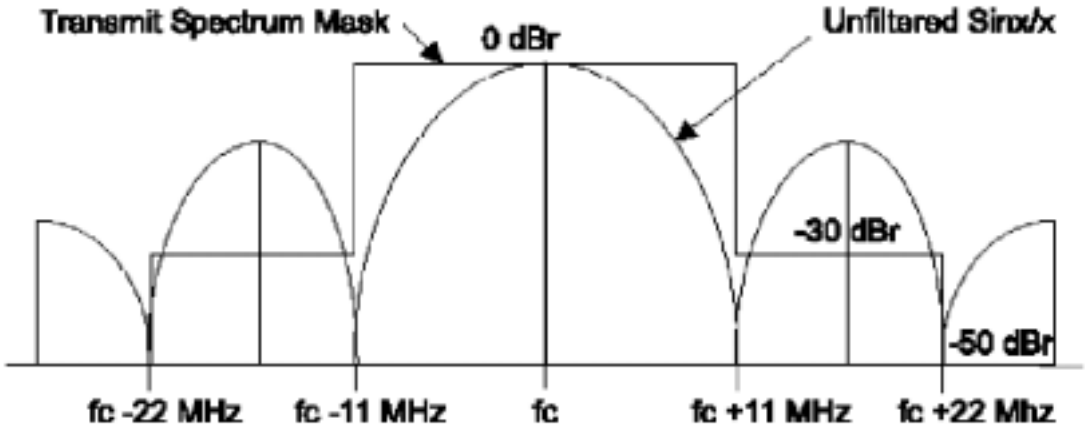


Figure 1-2 802.11b Transmit spectrum mask

accuracy shall be determined by measuring the peak error vector magnitude (EVM) during each chip period. The worst-case error vector magnitude shall not exceed 0.35 for the normalized sampled chip data, i.e., EVM has to be less than 35%.

1.1.2 IEEE 802.11a

802.11a defines the standard for wireless LAN's working around 5 GHz, which is called Unlicensed National Information Infrastructure (U-NII) band. In comparison to 802.11b, it employs a different multiplexing technique: orthogonal frequency division multiplexing (OFDM). The OFDM system uses parallel subcarriers to transmit and receive a single data stream [2,3]. It is robust against frequency selective fading commonly found in indoor environments. In 802.11a [3], each channel contains 52 subcarriers: 48 data carriers and 4 pilot carriers. The pilot signals are used to make the coherent detection robust against frequency offsets and phase noise. The subcarrier frequency spacing is 312.5 kHz, but subcarriers are overlapped with each other in an "orthogonal" way to efficiently use the available spectrum. To avoid difficulties in D/A and A/D converter offsets

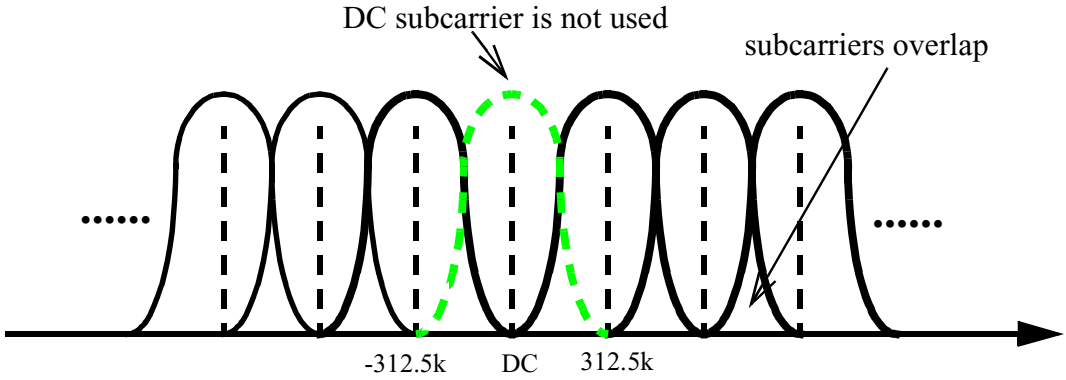


Figure 1-3 A simplified 802.11a OFDM system subcarriers frequency allocation

and carrier feedthrough in RF systems, the subcarrier falling at DC (0^{th} subcarrier) is not used. The subcarrier frequency allocation is illustrated in Figure 1-3.

In the United States, U-NII band includes three subbands: U-NII lower subband, from 5.15 GHz to 5.25 GHz; U-NII middle subband, from 5.25 to 5.35 GHz; and U-NII upper band, 5.725 to 5.825 GHz. The lower and middle U-NII subbands accommodate eight channels in a band with a total width of 200 MHz. The upper U-NII band accommodates four channels in a 100-MHz width band. The channel frequency spacing is 20 MHz and the occupied channel bandwidth is 16.6 MHz. The U-NII bands with channel locations are shown in Figure 1-4.

The OFDM system can support data rates of 6, 9, 12, 18, 24, 36, 48, and 54 Mbit/s. The support of transmission and reception at data rates of 6, 12, and 24 Mbit/s is mandatory. The system uses either binary or quadrature phase shift keying (BPSK/QPSK), 16-quadrature amplitude modulation (QAM), or 64-QAM, depending on the data rate. Forward error correction coding (convolutional coding) is used with a coding rate of 1/2, 2/3, or 3/4.

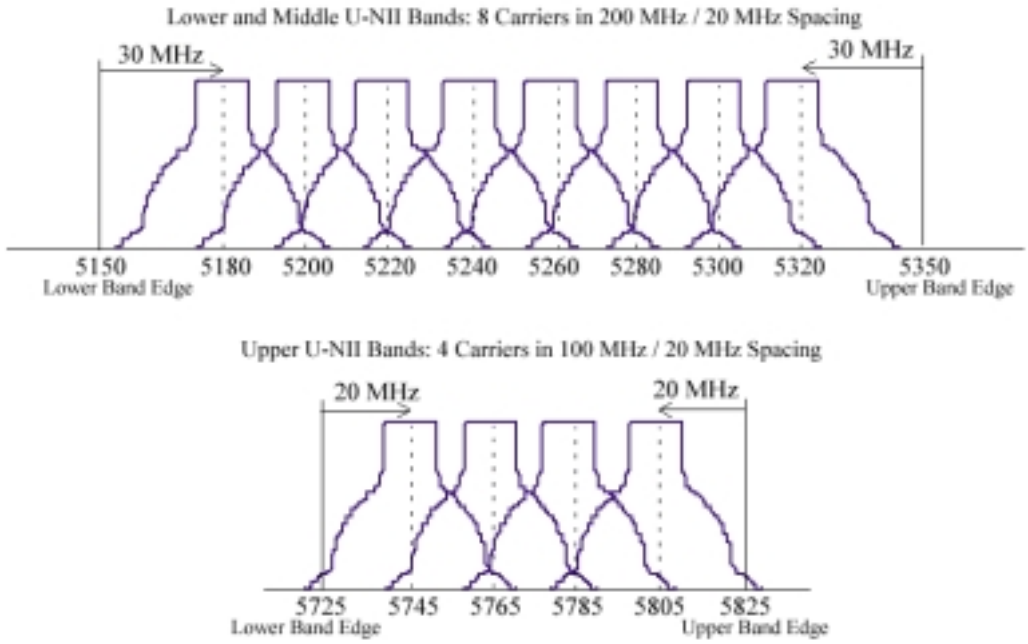


Figure 1-4 802.11a OFDM system channel frequency locations

The specified operating temperature range by the standard is 0 °C to 40 °C, for office environments (Type 1). Type 2, with a range between -20 °C and 50 °C, and Type 3, with a range between -30 °C and 70 °C, are designated for industrial environments.

Since the 802.11a OFDM system supports 8 different data rates, the receiver minimum input level sensitivities depend on data rates, and are listed in Table 1-1. The receiver shall provide the packet error rate (PER) less than 10% at a PSDU length of 1000 bytes for input sensitivities measured at the antenna connector.

The adjacent channel rejection test is performed by applying a -63 dBm conformant OFDM signal at an adjacent channel, unsynchronized with the signal in the channel under test, which is 3dB above the minimum sensitivity, as stated in Table 1-1. The receiver must maintain a maximum 10% PER at the output of the receiver. The alternate

Table 1-1Receiver performance requirement

Data Rate (Mbit/s)	Mini. Sensitivity (dBm)	Adjacent Channel Rejection		Alternate Adjacent Channel Rejection	
		Input signal (dBm)	Adj. CH. (dBm)	Input signal (dBm)	Alt. Adj. CH.(dBm)
6	-82	-79	-63	-79	-47
9	-81	-78	-63	-78	-47
12	-79	-76	-63	-76	-47
18	-77	-74	-63	-74	-47
24	-74	-71	-63	-71	-47
36	-70	-67	-63	-67	-47
48	-66	-63	-63	-63	-47
54	-65	-62	-63	-62	-47

adjacent channel rejection test is performed while applying the same signal in the channel under test. The signal power at an alternate adjacent channel is -47 dBm.

The maximum receiver input level is -30 dBm measured at the antenna for any baseband modulation. Under this condition, a receiver must maintain a maximum PER of 10% at a PSDU length of 1000 bytes.

The maximum transmit output power is 40 mW for the lower subband, 200 mW for the middle subband and 800 mW for the upper subband in the USA. The transmitted spectrum shall have a 0 dBr (dB relative to the maximum spectral density of the signal) bandwidth not exceeding 18 MHz, –20 dBr at 11 MHz frequency offset, –28 dBr at 20 MHz frequency offset and –40 dBr at 30 MHz frequency offset and above. The spectral density of the transmitted signal shall fall within the spectral mask shown in Figure 1-5.

The measurements shall be made using a 100-kHz resolution bandwidth and a 30-kHz video bandwidth.

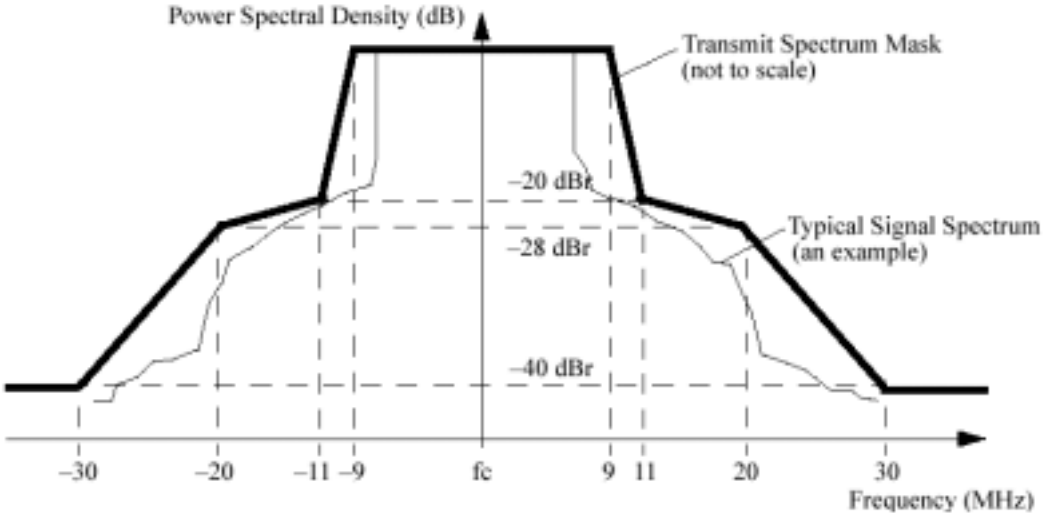


Figure 1-5 801.11a transmit output power mask

The transmit relative constellation RMS error, averaged over subcarriers, OFDM frames, and packets, shall not exceed -5 dB or -25 dB for data rate of 6 Mbit/s or 54 Mbit/s, respectively.

1.1.3 IEEE 802.11g

IEEE 802.11g is the 802.11a standard operating in the 802.11b band (2.4 GHz Industrial, Scientific and Medical band). IEEE 802.11a OFDM system has a higher maximum data rate (54 Mbit/s) than 802.11b (11 Mbit/s). But 802.11a has higher free space path loss than 802.11b because its operation frequency is higher than IEEE 802.11b. That means 802.11a has a shorter range compared to 802.11b for the same transmitted power. To support high data rate and a larger range at the same transmitted power, 802.11g standard operating at 2.4 GHz is defined. Many of 802.11b RF circuits are acceptable for those needed for 802.11g. The exceptions are the power amplifier (PA), voltage controlled oscillator (VCO) and RF switches.

1.1.4 HIPERLAN/2

All 802.11 standards listed above are for the USA and its territories. For countries or area outside of the USA, wireless LAN may or may not be compatible with the 802.11 standards. This thesis focuses on the applications in the United States. But it is worthwhile to briefly introduce another important wireless LAN standard: high performance local area network type 2 (HIPERLAN/2) standard. HIPERLAN/2 is used in Europe and its territories, and defined by the European Telecommunication Standards Institute (ETSI). HIPERLAN/2 is very similar to the IEEE 802.11a standard expect that operation frequency range is slightly different [4]. HIPERLAN/2 operates in two subbands from 5.15 to 5.35 GHz, and from 5.47 to 5.725 GHz. The OFDM system in HIPERLAN/2 is almost the same as that for 802.11a. HIPERLAN/2 also supports data rates up to 54 Mbit/s with 64-QAM modulation.

1.2 Wireless LAN IC Design Challenge

Since IEEE adopted the 802.11a/b standards in 1999, the 802.11 wireless LAN market has been enjoying exceptional growth. According to Callahan and Durand [5], 802.11 silicon shipments will reach 35 million chips in 2003. This is an 80% growth for the 2003 alone. As this trend continues, more and more companies have been entering this market. The intense competition drives the price down and leaves little room for profits. In terms of the implementation of wireless LAN RF circuitry, this trend limits the technology choice. Ultimately, only the low-cost CMOS technology is expected to be viable in this market. In comparison to other integrated circuits technologies like SiGe BiCMOS or GaAs, CMOS is still considered as a low performance “digital circuit” technology. Thus,

to achieve the required performance using a low-cost technology like CMOS is a challenge for WLAN IC designers.

Another WLAN IC design pressure is the rapid pace at which the market is evolving. The WLAN market is no longer to expected to be dominated by PC-based products alone. Increasingly, it will be co-driven by A/V and consumer-media devices, like flat-panel-TV screens, PDAs, gaming devices, and etc. Furthermore, it will be incorporated into cellular phones to provide high speed internet access. That requires WLAN based products not only mobile, but also easily carried (portable). The WLAN IC has to be smaller and lower power.

Like the other wireless systems, the co-existence of multi-standards operating at multiple frequency bands challenge RF circuit designers. There are already products now targeting multi-band WLAN applications. They however utilize multiple RF chains to support the multiple frequency band applications. This makes the chips and systems large and increases cost. The single chip tunable multi-band IC is attractive for its smaller area and lower cost.

1.3 Overview of the Dissertation

This Ph.D. work concentrates on the design issues of tunable multi-band CMOS receiver circuitries, as well as receiver system design approaches. The wireless LAN applications are used as the demonstration vehicle. The evaluation of feasibility for implementing a tunable multi-band multi-standard wireless LAN single chip receiver serves as the first step for someday realizing a tunable multi-band multi-function transceiver.

In Chapter 2, a tunable multi-band multi-standard receiver architecture for wireless LAN application is described. The key blocks are switches, a tunable multi-band RF/IF

down-converter, a multi-band voltage controlled oscillator (VCO) and a wide tuning range VCO. The whole receiver is intended for implementation as a single chip CMOS receiver. The 5.8 GHz and 2.4 GHz CMOS switches were first designed and tested. The measurements are presented in Chapter 3. In Chapter 4, a technique to improve CMOS switch power handling capability at high frequency has been demonstrated by implementing two 15-GHz CMOS switches. In Chapter 5, a VCO with a 54% tuning range, which satisfies the 802.11 phase noise specifications is described. By frequency dividing the VCO output by two, the quadrature signals for the second mixer of the receiver are generated. Chapter 6 and Chapter 7 demonstrated two multi-band circuit: Chapter 6 shows a multi-band VCO and Chapter 7 discussed a dual-band RF/IF down-converter. The multi-band VCO achieves four output frequency bands (2.4, 2.5, 4.7 and 5.0 GHz) with the lowest phase noise reported to data for CMOS VCO's in each respective band. A dual-band RF CMOS RF/IF down-converter incorporates a switched gain function besides the band selection. The tunable function is realized by using switched resonators. Chapter 8 discussed theoretical and experimental studies on the VCO injection locking. Lastly, a summary and suggested future works are presented in Chapter 9.

CHAPTER 2
TUNABLE MULTI-BAND WLAN RECEIVER SYSTEM

2.1 Introduction

The IEEE 802.11 wireless LAN standards are introduced in Chapter 1. Presently, there are numerous receiver architectures which can be used to implement the receivers for standards. For example, a WLAN receiver can be easily realized using a superheterodyne architecture [6] which is commonly used in modern communication systems. However the superheterodyne architecture may not be the best solution to accomplish WLAN circuits. An architecture needs to be chosen or designed before circuit implementation. The primary criteria for selecting a receiver architecture are the cost, power consumption, complexity and performance.

WLAN is a commercial application. A low price is the key for gaining market share. A single chip is cheaper than multi-chip solutions. For a single chip IC, there are three sources for cost: the chip fabrication cost, the cost of external components and the cost of assembly. To reduce cost, the chip area needs to be small, and the external component count should be reduced. Numerous applications of wireless LAN's are battery powered, and low power consumption of receiver circuits is critical. Design complexity is also an important consideration for selecting a receiver architecture. Compared with a simple system, a more complex system means more circuit components, thus more area and more power consumption. Also, a complex system requires more time to design. In order to hit a market window, a short design cycle is critical. So, a simpler system is preferred over a

more complex system if both can meet the standards. The last criterion for selecting a receiver architecture is the performance. The performance is mainly defined by the standards. The WLAN standards are targeting indoor applications and their range is only up to a couple of hundred meters. The wireless systems for commercial applications usually do not require as high performance as military applications. This gives more flexibility in receiver architecture selection.

This chapter reviews some common receiver architectures (section 2.2.) including the trade-offs and design issues of these architectures. In section 2.3, a dual-conversion zero IF receiver architecture chosen for the tunable multi-band multi-standard single chip WLAN CMOS receiver is presented.

2.2 RF Receiver Architecture Overview

2.2.1 Superheterodyne Receiver

Since it was invented by Edwin H. Armstrong in 1918, the superheterodyne receiver has been widely used in RF wireless systems such as AM/FM radio, television, satellite, and others [6]. This technique frequency translates an incoming RF signal to a convenient frequency band, called the intermediate frequency (IF) band, and then extracts the information by using an appropriate demodulation scheme. A simple superheterodyne receiver block diagram is shown in Figure 2-1.

There are three filters in the superheterodyne receiver. The first one can be either a simple band pass filter (BPF) or a duplexer, depending on multiple access techniques (e.g. time division or frequency division). Both BPF and duplexer select only the band of interest and reject out-of-band interferers. An image reject filter enhances the band selection function and provides additional suppression (typical ~60 dB) for the out of band image

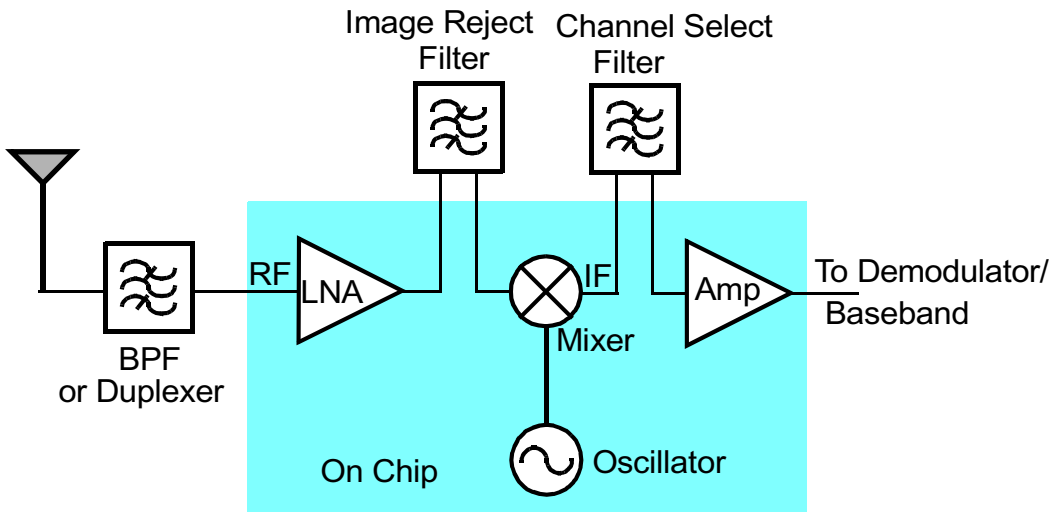


Figure 2-1 Simple superheterodyne receiver

signal. After the mixer, the signal at RF is translated to IF which is typically 5 to 10 times lower than the RF frequencies. Thus, the channel select function is possible at a low intermediate frequency, which is fixed. In contemporary communication systems with radio frequencies (RF) in the GHz range, these three filters have to be off-chip as illustrated in Figure 2-1. This significantly increases bill of material (BOM). Driving off-chip filters also raises power consumption since the interface between on-chip and off-chip is 50 Ω, which is significantly lower than the on-chip impedance levels. The payback of the off-chip filters is their high selectivity. This makes the superheterodyne receiver high performance and easier to implement. Since these filters are off-chip, they can be redesigned or replaced after circuit implementation. So, it is also easier to fix design flaws for a superheterodyne receiver.

In a nutshell, a superheterodyne receiver has better performance and is suitable for discrete circuit design. But its higher component count makes it less attractive for commercial products where cost is of the utmost importance.

2.2.2 Image-Rejection Receiver

The image rejection receiver architecture used in modern communication systems fits better with the integration trend. As the device technology based on silicon continues to advance, the chip fabrication cost becomes a small portion of the total bill of material (BOM). Off-chip components like filters may cost as much as 20 – 30% of die cost. The image rejection receiver provides image rejection on chip, thus image reject filter is no long needed.

There are two types of image-reject receiver architecture [7]: Hartley architecture and Weaver architecture. Both utilize quadrature signals in conjunction with addition or subtraction at the output. The image is cancelled, while the desired signal is preserved. The mathematics treatments of how these architectures work can be found in Razavi [7].

The image-reject receiver architecture increases the number of on-chip circuits to lower the number of off-chip filters. Figure 2-2 shows a simple Weaver image-reject receiver. It needs four mixers, two low pass filters (LPF's) and one subtraction function

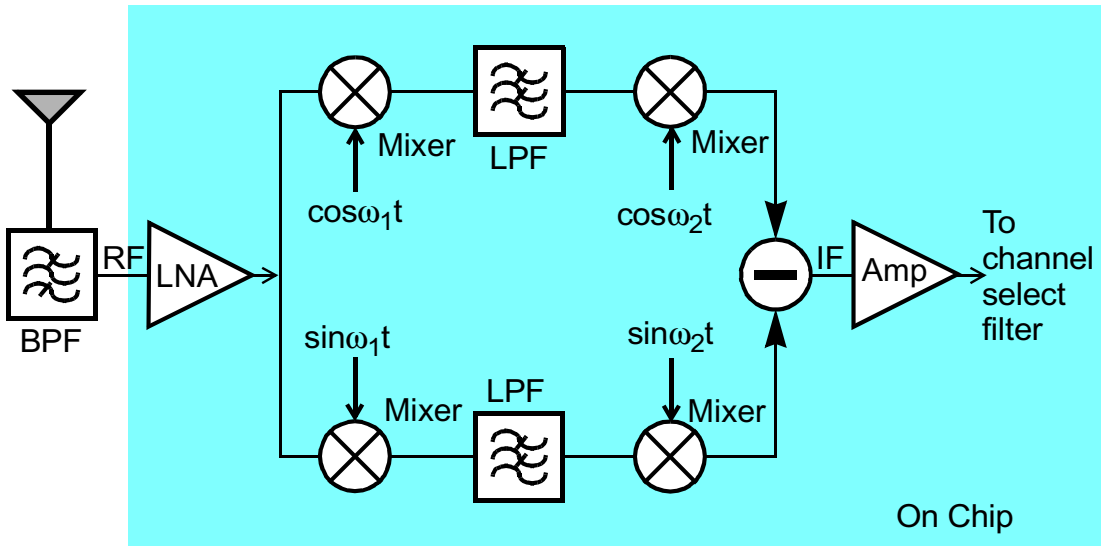


Figure 2-2 Simple Weaver image-reject receiver

instead of one mixer and one filter in a superheterodyne architecture receiver. This does raise power dissipation and chip area.

The image rejection ratio of an image-reject receiver depends on phase and amplitude matching. If phase accuracy and amplitude balance are perfect, the image will be blocked totally. But in reality, without careful design, the matching can be poor in integrated circuits. An image rejection ratio of 40 dB has been reported in Wu and Razavi [8].

Though an image-reject filter is eliminated in an image-rejection receiver, the channel select filter is still needed after the down-conversion to IF. Since BPF provides image rejection as well, the image-reject filter can be a relatively low Q (filter quality factor) LC filter, which is inexpensive. But the channel select filter in most cases needs high Q and is implemented with a surface acoustic wave (SAW) filter. SAW filters have the highest Q but are more expensive. The motivation to integrate the channel select filter on-chip led to alternative receiver architectures. One of them is the low-IF receiver architecture.

2.2.3 Low-IF Receiver

The low-IF receiver utilizes a low intermediate frequency (IF), where the channel select function can be realized by using on-chip active filters. But low intermediate frequency means the desired signal and image signal are placed very close to each other. It requires an ultra high Q image reject filter, which is costly. So other techniques are needed to suppress the image signal.

The image problem present in traditional superheterodyne receivers is illustrated in Figure 2-3 (a). The down-conversion is accomplished by multiplying a sinusoidal signal with the incoming signal. In frequency domain, this is represented by a two delta func-

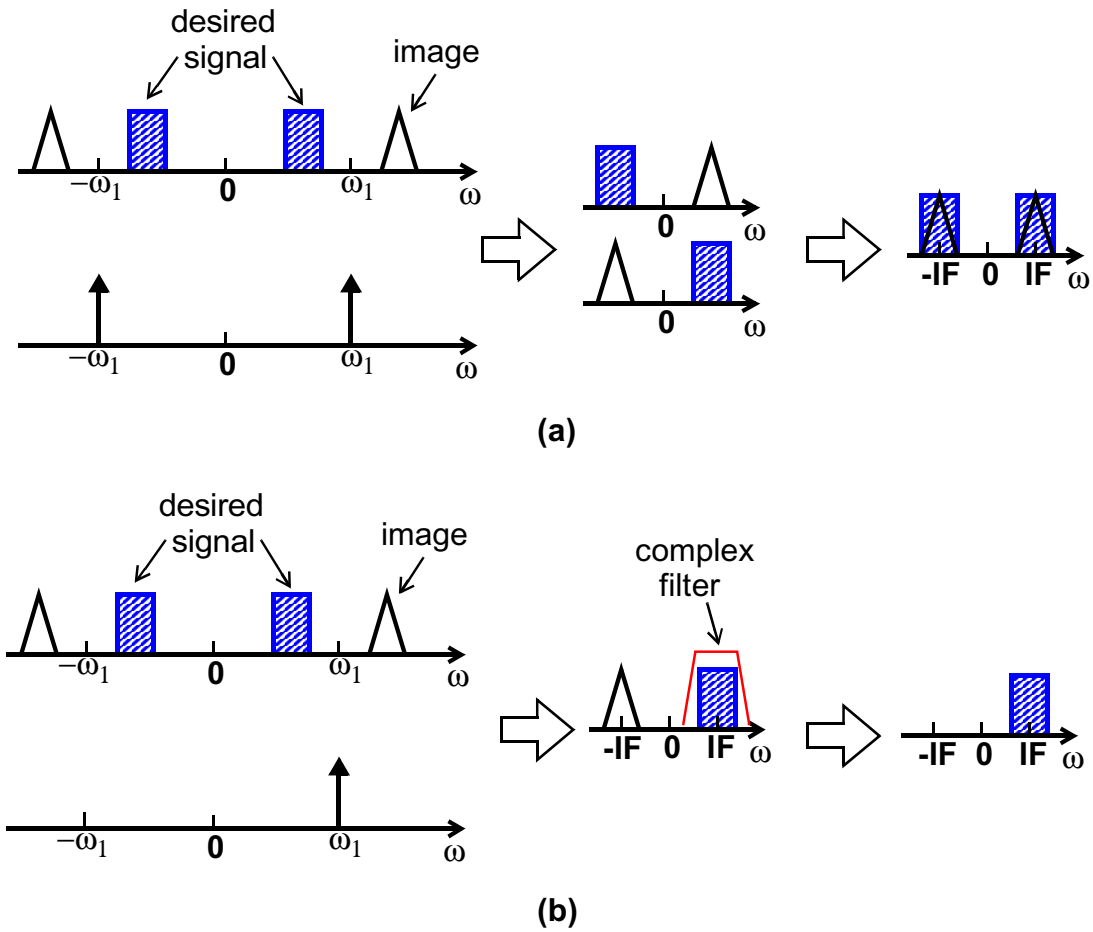


Figure 2-3 The IF down-conversion process in (a) a superheterodyne receiver. (b) a low-IF receiver

tion in positive and negative frequency. During the down-conversion, multiplication with a positive frequency signal moves the image and desired signals with negative frequencies toward the right; multiplication with a negative frequency signal moves the image and desired signals with positive frequencies toward the left. The result is that both the image and desired signals are present at the positive frequency side, and both the image and desired signals are present at the negative frequency side. They are combined in such a way that can not be separated by any filtering techniques as shown in Figure 2-3 (a).

During the down-conversion, if a single positive frequency signal is used, then the desired signal can be placed in the positive axis and the image signal can be placed in the opposite frequency in the negative axis as illustrated in Figure 2-3 (b). They are not superimposed. In this case, complex filtering which suppresses the signals in the negative frequency axis can be applied to separate wanted signal and image signal [9]. As shown in Figure 2-3 (b), this image rejection occurs at the intermediate frequency.

A quadrature down-converter generates a single positive frequency signal. A quadrature down-converter has been extensively used in direct converter receivers, which will be discussed in the next subsection. The difficulty associated with a quadrature down-converter is that the image rejection depends on precise matching and phase accuracy of the quadrature signals. Use of the quadratures with phase/amplitude errors generates signals at negative frequencies. As seen in Figure 2-3(a), the negative frequency signals will cause some portions of the image signals to be superimposed with the desired signals, and they can not be separated by a complex filter. “Depending on applications and the exact position of IF, the image can be up to 20 dB higher than the wanted signal, resulting in a required phase accuracy of 0.3°” [9]. This accuracy, with today’s typical quadrature down-converters, can only be achieved with the use of extensive tuning and trimming. So an implementation with better image rejection is necessary.

Such a receiver is shown in Figure 2-4 [9]. A double quadrature down-converter with a low IF receiver architecture is illustrated. A polyphase filter after the LNA is for additional image reject. As seen from Figure 2-3(b), the image signal located at -IF after down-conversion which is from the image at negative frequency, i.e., the image signal around $-\omega_1$. So, the polyphase filter only needs to suppress this portion of the image sig-

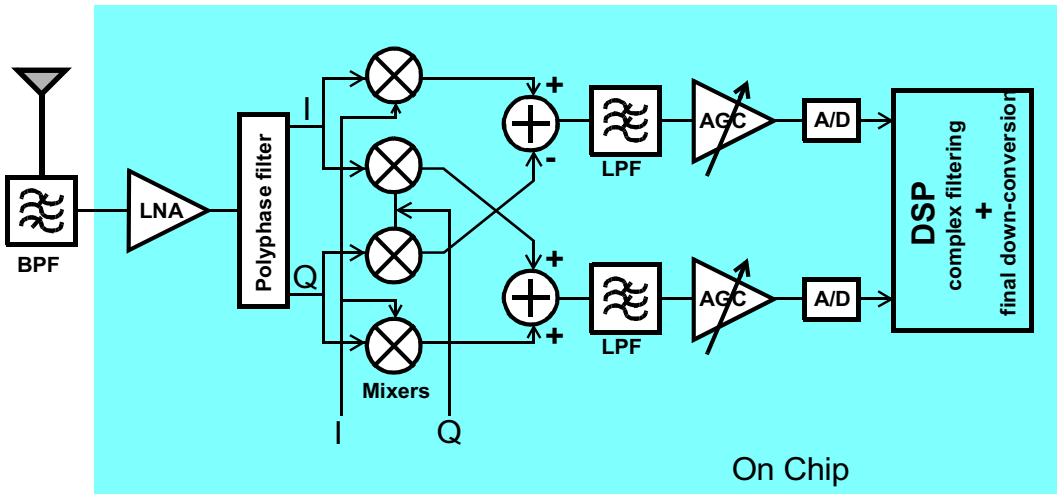


Figure 2-4 Low IF receiver

nal. It is not necessary to suppress the image signal at both the positive and negative frequencies. The suppression of only the negative frequency components does not require a high Q filter. Consequently a I, Q-signal pair is generated after the polyphase filter, so a double quadrature down-converter with four mixers is placed after the polyphase filter. The double quadrature down-converter is shown to be much less sensitive to the inaccuracies of the phase and the imbalances of the amplitude of the RF and LO inputs to the mixers [10].

The complex filtering can be performed either in analog or digital domain [9]. If analog signal processing is used, a polyphase filter can be placed after the down-converter to suppress the image. The signal is digitized using an A/D converter after the polyphase filter. But with today's A/D-converters, it is possible to sample the low frequency signal before the image signal has been suppressed. This is shown in Figure 2-4. The image suppression filtering and final down-conversion are now done in a digital signal processor (DSP) with better accuracy.

The low IF receiver shows the potential for a higher level of integration, which could lower the cost. But the polyphase filter and double down-converter require more power consumption to compensate the filter loss and to drive the four mixers. Another relative simple architecture with a high level of integration is the direct conversion receiver architecture. Though, a direct conversion receiver requires fewer circuits than low IF receivers, it has some design difficulties. This is addressed in next section.

2.2.4 Direct Conversion Receiver

The direct conversion receiver is shown in Figure 2-5. The direct conversion architecture can be treated as a special case of a low IF receiver architecture with IF approaching to zero. The down-conversion is still by the means of multiplications with a positive frequency, as illustrated for the low IF receiver architecture. But in direct conversion receiver, the mirror signal (called image signal in the low IF architecture) is the desired signal itself, thus the 25 dB mirror signal suppression is suffice for most applications [9]. So, only a quadrature down-converter is needed in a direct conversion receiver instead of a

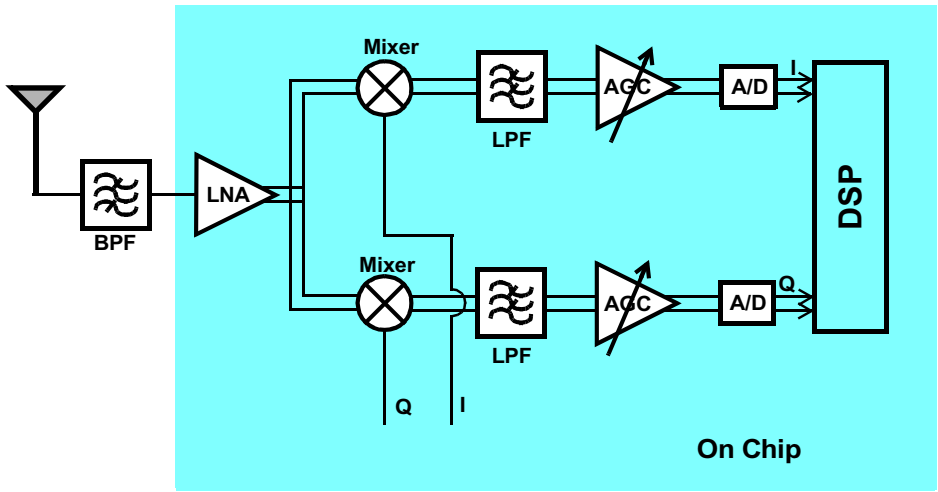


Figure 2-5 Direct conversion receiver

double quadrature down-converter and a polyphase filter in a low IF receiver. A direct conversion receiver is also called a zero IF (ZIF), homodyne or synchrodyne receiver [6].

The advantages of a direct conversion receiver is obvious: it is simple and almost all of the receiver can be integrated. One quadrature down-converter directly translates the band of interest to zero frequency, which also performs part of demodulation. Because of this, it is called quadrature demodulator. A low pass filter (LPF) selects the channel and suppresses nearby interferers, and no external SAW filter is needed. An automatic gain control (AGC) amplifier boosts demodulated signal power at zero frequency before it is sampled by an A/D converter. It is simpler with a fewer circuits. It occupies a smaller area and costs less. But the design of a direct conversion receiver is considered challenging. The reason is that direct conversion receiver has several design issues or difficulties which may not associate with the superheterodyne, image-rejection, or low-IF receivers. Those drawbacks are dc offset, I/Q mismatch, even-order distortion, flicker noise and oscillator leakage [11].

The DC component is generated if the signal frequency at mixer input is the same as the signal frequency at mixer LO port. Four of the possible paths which could cause DC offset is shown in Figure 2-6. Figure 2-6(a) illustrates two paths for the LO signal to appear at the mixer input: the LO signal could leak into the LNA input, and after the LNA amplification, it reaches the mixer input; or the LO signal is directly coupled to the mixer input through the substrate and due to the finite LO-RF isolation. This phenomenon is called self-mixing. A similar effect can occur if a large interferer leaks from the LNA or mixer input to the LO port and is multiplied by itself, as shown in Figure 2-6(b). The fourth path is associated with LO leakage to the antenna. Since for a direct conversion

receiver, LO frequency falls in the interested channel band, the BPF or tuned LNA circuits do not reject this. LO could leak to the antenna with an unacceptable power level. It is radiated and subsequently reflected back from objects in the surrounding to the receiver. Then, this generates DC offset varying with time as illustrated in Figure 2-6(c). The DC offset is problematic in a direct conversion receiver since it is generated by in-band signals. In a direct conversion receiver, the wanted RF signal is down-converted to DC. This is not the case in other types of receivers like a superheterodyne receiver. In a superheterodyne receiver, DC offsets fall out of the frequency bands for desired signals and can be easily filtered [11].

The second design issue in a direct conversion receiver is I/Q phase accuracy and amplitude mismatch. As mentioned, in the context of a low-IF receiver, the perfect quadratures generate a single positive frequency signal. If there are large components at negative frequency which are associated with unbalanced quadratures, the image rejection ratio will be low. The I/Q phase accuracy and amplitude matching always become worse as frequency is increased. At low frequencies, large devices can be used to improve matching. And it is less sensitive to interconnection parasitics mismatch because the

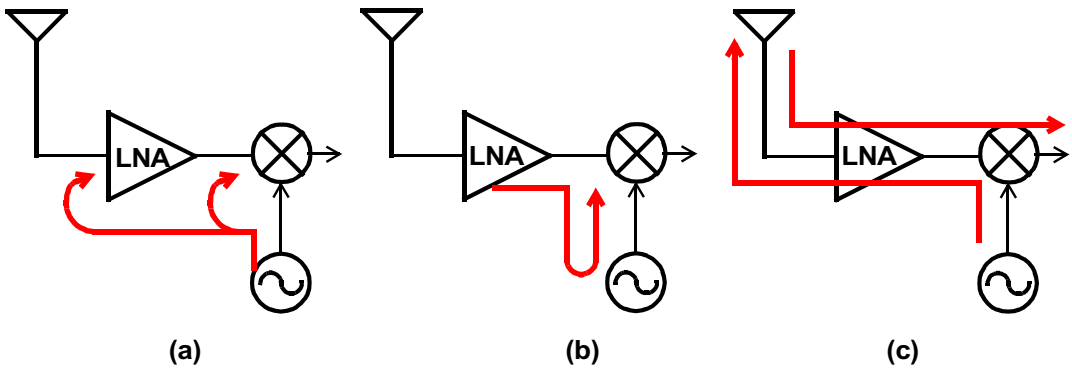


Figure 2-6 Paths to generate DC offset in direct conversion receiver: (a) LO self-mixing, (b) RF self-mixing, (c) LO leakage to the antenna then reflect back

capacitance and inductance from circuits are larger. WLAN applications using OFDM require more strict I/Q control.

The third issue in direct conversion receivers is even-order distortion. Even-order distortion, such as the second order distortion, will generate intermodulation products around DC thus falls into the signal band. This is not a problem if IF frequency is away from DC. The fourth issue is the flicker noise. Flicker noise is a "colored noise" and increases when the frequency is decreased. This is particularly severe in a MOS device due to the proximity of a channel to a Si/SiO_2 interface. The total noise figure is degraded and the information close to DC could be swamped out by the flicker noise. The last design issue for a direct conversion radio is LO leakage to the antenna. As mentioned in the context of DC offset problem, there is no filtering for an LO signal in a receiver chain. An LO signal could reach the antenna and radiate at a power level higher than that required by FCC regulations [11].

Both direct conversion and low IF receiver architectures can have a high integration level which the superheterodyne and image-reject receiver can not. But both the direct conversion and low-IF receiver require precise control of I/Q phases and amplitudes. This is a serious challenge for 5-GHz WLAN implementation, where the operation frequency is high.

One way to alleviate the matching problem is to use two-step conversion, i.e., to convert RF to first IF, then use either low IF or direct conversion architecture after that. The first IF will be much lower than RF so the matching and quadrature phase control is relative easy to achieve. The image caused by the first IF can be rejected by the bandpass filter succeeding the antenna in WLAN application as we will see in the next subsection.

A low IF receiver is more complex than a direct conversion receiver with more circuits, a larger area and higher power consumption. Though, direct conversion has many draw-backs, those issues can be remedied in integrated circuits with careful system and circuit design. Based on this, a dual-conversion zero IF receiver architecture is proposed for multi-band multi-standard WLAN CMOS receiver. Its design issues like DC-offset, image rejection, etc. are discussed in next section.

2.3 Proposed Tunable Multi-band Receiver System

2.3.1 A Multi-band Dual-Conversion Zero IF Receiver

The block diagram of proposed single chip multi-band receiver is given in Figure 2-7. Two sets of antennas and band pass filters are used for 2.4GHz and 5GHz WLAN bands. Since WLAN's employ time-division duplex, a T/R switch is needed to multiplex the use of antennas by a receiver and transmitter chain. A diversity switch is not included in the system block diagram because the diversity antenna is not part of the IEEE 802.11

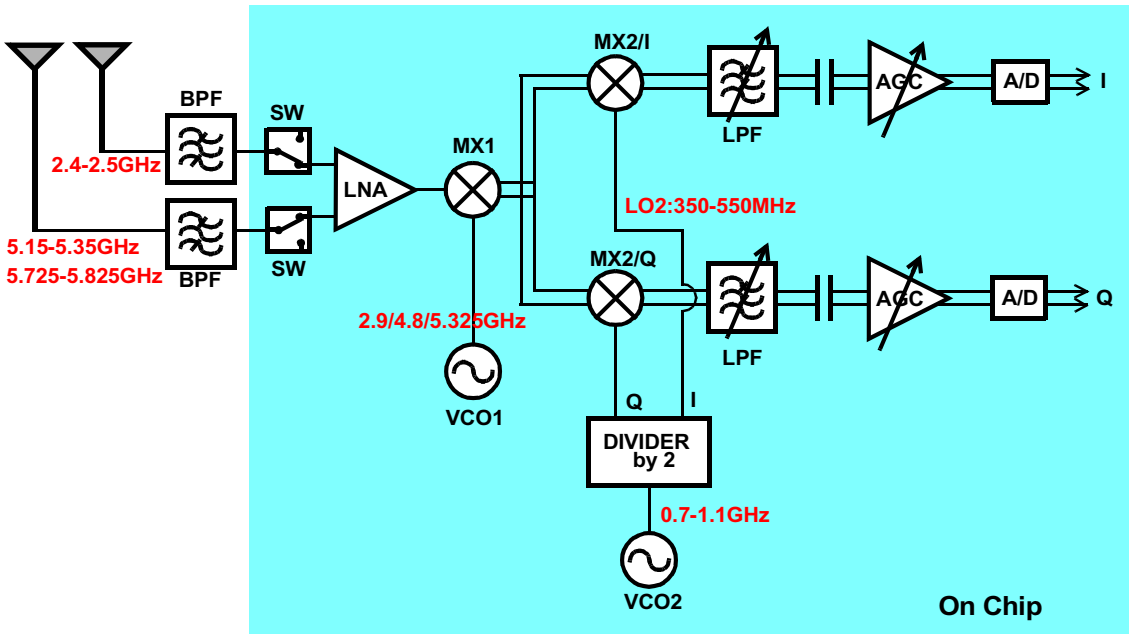


Figure 2-7 Proposed multi-band single chip dual-conversion zero IF receiver block diagram

standard requirement. The diversity switch design is covered in Chapter 3. Including the T/R switches, all circuits after BPF are planned to be integrated into a single chip as shown in Figure 2-7.

The receiver has two inputs, one for the 2.4GHz band and another for the 5GHz band. Corresponding to this, there are two T/R switches planned for the chip: a 2.4 GHz switch and a 5-6 GHz switch. A multi-band low noise amplifier (LNA) handles two outputs from switches. The band selection is accomplished by a multi-band LNA. Since 802.11a/b/g are standards for the same application, just at different bands, it is assumed that a radio does not need to simultaneously operate at the both frequency bands. Having this band selection greatly reduces the cross-talk between bands and makes the receiver implementation easier. For example, one scenario for receiver failure is that when a radio is receiving a high data rate signal near its sensitivity in the 5GHz band, if the 2.4GHz band signal is strong, then to detect the wanted 5GHz signal, AGC and LNA all should be at their maximum gain status. If there is no band selection in the radio, depending on how gain and linearity are distributed along the receiver chain, a 2.4-GHz signal which is as little as 10 – 20 dB higher than the 5 GHz signal can saturate the receiver and cause the whole radio to malfunctions.

The LNA output is connected to the first mixer input (MX1 in Figure 2-7). The MX1 LO ports are driven by a multi-band voltage controlled oscillator (VCO1 in Figure 2-7). The LO frequency is set such a way that their first intermediate frequencies are located close to each other. A detailed frequency plan is given in subsection 2.3.2. A quadrature down-converter follows MX1. It includes MX2/I and MX2/Q which are driven by quadrature LO signals. The quadrature LO signals are generated by the second VCO

(VCO2) and divide-by-2 circuit. The quadrature down-converter translates the signals at the first IF to either second IF or DC. From here the receiver is divided into two paths, one for the in phase (I) signal and the other for the quadrature (Q) signal. Both paths are composed of a low pass filter (LPF), an ac coupling capacitor and an automatic gain control amplifier (AGC).

LPF performs the channel selection. Since the desired signals are now located from DC to ~10MHz, it is straight forward to implement an integrated active LPF for such purpose [12]. When an active filter is used, part of the gain control function can be incorporated into the filter. An AC coupling capacitor is used to remove the DC offset. The AGC is an amplifier with varying gain to improve the receiver dynamic range. The 802.11b standard requires a minimum sensitivity of -76 dBm (see Chapter 1 for standards). For contemporary A/D converters, their inputs are about 0.5 to 1V peak to peak. That sets the required maximum voltage gain of receiver chain as ~80dB. Assuming the gain from LNA and mixers (MX1 and MX2) are ~30 dB, the total gain needed from LPF and AGC is ~50dB.

2.3.2 Receiver Frequency Plan

The receiver is designed for IEEE 802.11a/b/g standards. The bands need to be covered are 2.4 – 2.5 GHz, 5.15 – 5.35 GHz and 5.725 – 5.825 GHz. In this dual-conversion receiver, a wide-band IF technique is utilized [13]. For a wide-band IF receivers, the VCO frequency is fixed for the desired band, so the wanted channel is not centered around an IF frequency. The wanted channel is centered around a fixed frequency by the second conversion. For example, for 2.4 – 2.5 GHz band, the VCO1 output is fixed at 2.9 GHz. If the wanted signal is 2.437 GHz, then VCO2 has to be 463 MHz to down convert and cen-

ter the wanted signal at DC. Because of this, the VCO2 must have a wide tuning range. The reason for using this technique is to lower phase noise of VCO1.

WLAN applications, especially OFDM based systems require ultra low close-in VCO phase noise, i.e., the phase noise at a 10-kHz offset has to be -75 – -85 dBc/Hz. This type of phase noise has not been reported for integrated 5-GHz CMOS VCO at the time when the system was designed. To relax the VCO1 design requirement, the tuning range of VCO1 is scarified, i.e., as mentioned, its frequency is fixed. In VCO design, there is a trade-off between a VCO tuning range and phase noise due to the degradation of phase noise with increased VCO gain needed for a larger tuning range. The phase noise and tuning range of two required local oscillators can be traded-off in a dual-conversion system. The multi-band VCO is required to run only at a fixed frequency in each band, thus the tuning range of the first VCO can be traded-off for lower phase noise. At lower operating frequencies, lower phase noise can be traded for a larger tuning range. The second LO output frequency range is between 350 and 550 MHz. Since it operates at lower frequencies, the VCO can have excellent phase noise performance even with a wide tuning range. Additionally, having a fixed frequency in each band allows use of a phase locked loop with a wide bandwidth to further reduce phase noise [13]. So, with the wide-band IF architecture, it should be possible to integrate VCO1 with excellent phase noise performance.

The multi-band VCO (VCO1) needs to output tones at 2.9, 4.8 and 5.325 GHz. Thus, the first intermediate frequencies range from 350 to 550 MHz depending on the bands. The desired band, VCO1 output tones, IF and image frequencies are summarized in Table 2-1 for the multi-band WLAN receiver.

Table 2-1 The frequency plan of multi-band WLAN receiver

Band (GHz)	LO (GHz)	IF(MHz)	Image (GHz)
2.4 – 2.5	2.9	400 – 500	3.3 – 3.4
5.15 – 5.35	4.8	350 – 550	4.25 – 4.45
5.725 – 5.825	5.275	450 – 550	4.725– 4.825

The image rejection of first IF relies on the BPF, and the selectivity of antennas, LNA. In WLAN applications, image rejection requirement is not stringent. For example, IEEE 802.11a sensitivity is -65 dBm for 54 Mbit/s data rate. If BPF provides 60 dB image rejection and the antenna, LNA give additional 20 dB, the image with power of 0 dBm will not cause problems. A 0 dBm signal at the antenna port is considered as an extremely large signal.

The 60 dB image rejection of BPF is feasible using an off-chip filter with a notch near the image frequencies. A typical off-chip band pass filter [14] transfer function is plotted in Figure 2-8. The difference between the passband and notch band attenuation is

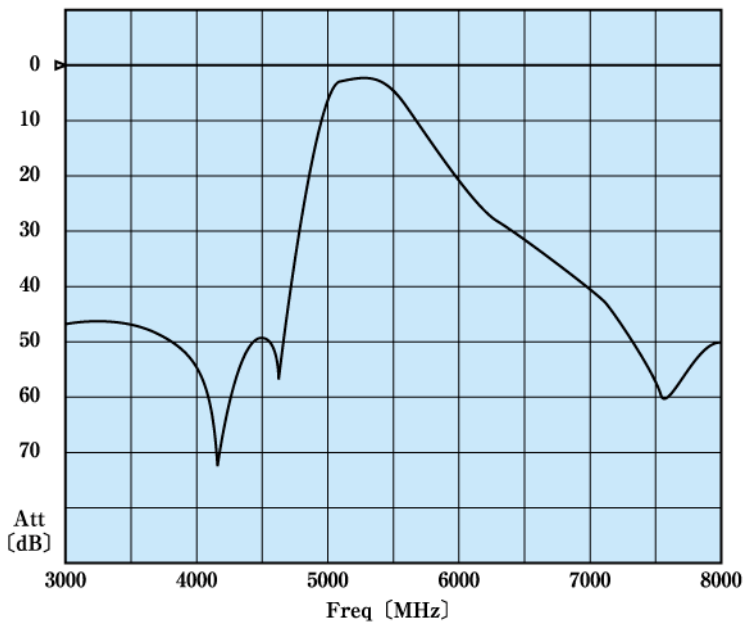


Figure 2-8 A typical band pass filter transfer function

over 70 dB, which satisfies the image rejection requirement.

From Table 2-1, there may be a problem if 5.15 – 5.35 and 5.725 – 5.825 GHz bands share a same bandpass filter. The images from the 5.725 – 5.825 GHz band are located at 4.725 – 4.825 GHz and are close to the passband of 5.15 – 5.35 GHz. But in case the BPF provides inadequate image rejection, this problem can be solved by adding another switch and a BPF for the 5.725 – 5.825 GHz band. Another possible solution is to increase the LO frequency to 6.725 GHz and move the image to 6.725 – 6.825 GHz. But this will make the design of multi-band VCO (VCO1) more difficult. The feasibility study of multi-band VCO (VCO1) uses the frequency plan given in Table 2-1.

The second conversion translates the signals at the first IF's to the second IF's which is DC. So, the quadrature down-converter needs LO frequencies between 350 and 550 MHz. A divided-by-2 circuit is used to generate the quadrature signals. Thus, VCO2 runs from 0.7 – 1.1 GHz as shown in Figure 2-7. This corresponds to a 45% VCO tuning range which is large.

The LPF selects a desired channel and rejects undesired spurs from the preceding down-conversion operation. The channel bandwidth is slight different among the IEEE WLAN standards. For example, the null-to-null channel bandwidth is 22MHz for 802.11b and the occupied bandwidth is 16.6 MHz for 802.11a. The active filter bandwidth can be made adjustable. Thus, all the standards can share the same active low pass filter. The LPF bandwidth needs to be as accurate as possible. If the bandwidth is lower than the required channel, the part of useful information is lost. If the bandwidth is too large, the larger noise bandwidth and insufficient filtering degrade the receiver sensitivity.

2.3.3 Design Issues

The dual-conversion receiver described above uses direct conversion for the second down-conversion. As mentioned earlier, the dual-conversion is used to mitigate the I/Q matching and phase accuracy requirements in direct conversion radios. But, this is not the only benefit for the proposed receiver. All the design issues with a direct conversion receiver can be alleviated or solved in this dual-conversion zero IF receiver.

LO leakage to the antenna is no longer a problem because two LO frequencies fall out of the BPF passband. LO frequencies will not be in the band which the antenna is tuned to. So, both the BPF and antenna provide rejection of LO signals. Without a large LO signal leaking to the antenna, the DC offset path in Figure 2-6(c) is no long a problem. LNA and MX1 are tuned for different frequencies than LO2 frequencies, which are the outputs of divider. Only two paths could generate DC offset in the dual-conversion receiver: the divider output is coupled to MX2 input and mixed with itself; and the MX1 output is coupled to MX2 LO port and self-mixed. But, isolating dividers is easier than isolating the LC tuned VCO because the divider's loads are resistors instead of inductors in an LC VCO. On-chip inductors occupy a larger area and it is one of the main paths for unwanted signal coupling.

The DC offset fails the radio by saturating a receiver with high baseband amplification. For example, if a 10-mV DC offset is created after MX2, then with the 50-dB gain from the LPF and AGC, it is 3.16 V at the input of A/D converter. This is too large for most A/D converters. In order to further suppress DC offset, an AC coupling capacitor is inserted between the LPF and AGC. Coupling capacitors block DC components. Assuming 20-dB gain from the LPF, a 10-mV DC offset from MX2 will be 100 mV at the filter

output. It is straight forward to attain V_{1dB} higher than 100 mV. Here V_{1dB} is the voltage of the circuit gain 1dB compression point. The AC coupling capacitor is a practical solution because WLAN systems have a wide bandwidth. In 802.11a standard, the subcarrier around DC is not even used. Considering the AC coupling capacitor as a high pass filter, the filter 3-dB frequency should be ~ 100 kHz, which can be integrated. With this AC coupling capacitor in place, the settling time needs to receive more attention in circuit design. It takes longer time to charge a large capacitor. When a WLAN system switches between the receiving and transmitting modes, the settling time requirement has to be met.

Even after adding the AC coupling capacitors, if the DC offset is still a problem, the DC offset cancelling techniques can be used. These techniques are proven to be effective to reduce the offset to less than 1 mV [15].

The dual-conversion allows a conversion to zero to occur at lower frequencies. At lower frequencies, larger device sizes can be placed to improve matching. Also the phase errors from VCO2 and the divider are smaller at lower frequencies. For example, if the phases of divider outputs deviates from a quadrature by 2 pico seconds. At 5GHz, this is 5GHz x 2 ps x 360° = 3.6° phase error. But at 500 MHz, it is only 0.36° phase error, which is more than acceptable.

The even oder distortion is one of the problems which can be solved with integrated circuit techniques. A common way to suppress even order distortion is to use a differential circuit topology. Differential circuits doubles the number of transistors. In the discrete circuits implementation, this is shunned because of an increase of component count and the difficulty in achieving adequate matching. But with integrated circuits design, this only increases chip area slightly and the transistor pair matching is signifi-

cantly better. The ideal differential topology is immune from even order distortion and rejects even order noise. Many circuits in integrated circuits use a differential topology: double-balanced mixer, operation amplifier, g_m cell, LC tuned VCO, and source-coupled logic (SCL) divider. The widely used differential circuits are appealing not only to direct conversion receiver, but also to superheterodyne and image-reject integrated receivers.

In order to convert a single-ended signal from an antenna to a differential signal, a balun is usually placed before the LNA in direct conversion receivers. Unfortunately, the loss of the balun directly raises the overall receiver noise figure. But in the dual-conversion receiver, the LNA is single-ended and MX1 acts as a single-ended to differential converter. There is no additional circuit needed thus there is no effect on overall noise figure. The blocks following MX1 are differential. This also helps with DC offset suppression because DC offset is an even order distortion.

MX2 is planned to be a passive mixer. The passive mixer do not have drain current and is free of flicker noise [16]. Flicker noise increases with decreasing frequency, and it is negligible at high frequencies ($f > \sim 10$ MHz). The frequency where the flicker noise is equal to white noise floor is called the corner frequency. When the frequency is below the corner frequency, flicker noise rise approximately -10 dB/decade. One way to circumvent the flicker noise is to have significant gain before the final conversion to DC. The noise floor of receiver after down-conversion is raised by the power gain, and the noise figure of RF and down-conversion stages, and the corner frequency is reduced [17]. For example, assume baseband circuits with 10-MHz corner frequency is realized in a CMOS technology. If the RF and down-conversion stages provide a power gain of 25 dB and a noise figure of 5 dB, the noise floor is raised by 30 dB relative to the thermal noise floor and the

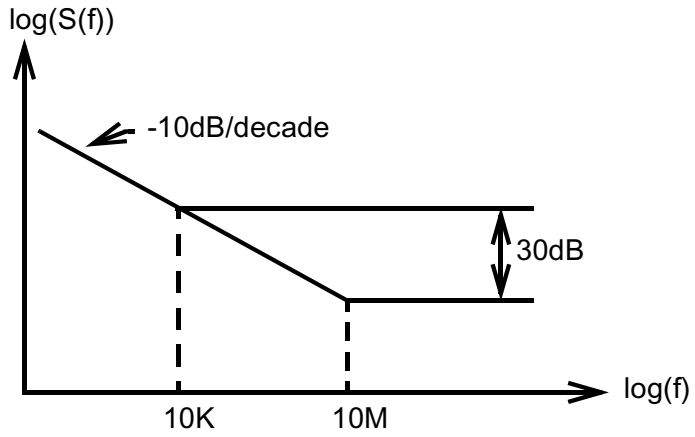


Figure 2-9 The baseband corner frequency decreases as the RF stage gain and noise figure increase

corner frequency is reduced by 30 dB to 10 kHz as illustrated in Figure 2-9. This corner frequency is much smaller than the WLAN channel bandwidths.

The high front-end gain is easily achieved in the dual-conversion receiver. The LNA and MX1 could provide voltage gain higher than 30 dB. But with only the LNA as a gain stage before the down-conversion in a direct conversion receiver, another gain stage is needed after the LNA (or called it two-stage LNA), even though, the amplification at RF is not power efficient.

Overall, the design challenges for a direct conversion receiver are not as severe in the dual-conversion zero IF receiver. The proposed receiver is a possible way to implement a highly integrated single chip tunable multi-band receiver.

CHAPTER 3
CMOS SWITCHES FOR WLAN APPLICATIONS

3.1 Introduction

A switch is usually the first circuit building block in a TDD (Time Division Duplex) communication system, in which transmission and reception occur at different time slots. A single pole double through (SPDT) switch used to share an antenna by the receive and transmit chains is called a Transmit/Receive (T/R) switch. In addition to it, for WLAN applications, there is another type of switches — diversity switch. In indoor environments, signals propagate typically through fading multipath channels. Two antennas are commonly employed to mitigate the problems arising from this. When a transceiver receives signals, the diversity switch chooses one of the antennas which has a stronger signal level. A single band WLAN transceiver is shown in Figure 3-1. It includes two antennas, a diversity switch, a BPF and a T/R switch.

The figures of merit for RF switches are insertion loss, isolation, return loss, P_{1dB} and IP_3. Insertion loss and isolation describe how much power can be delivered from

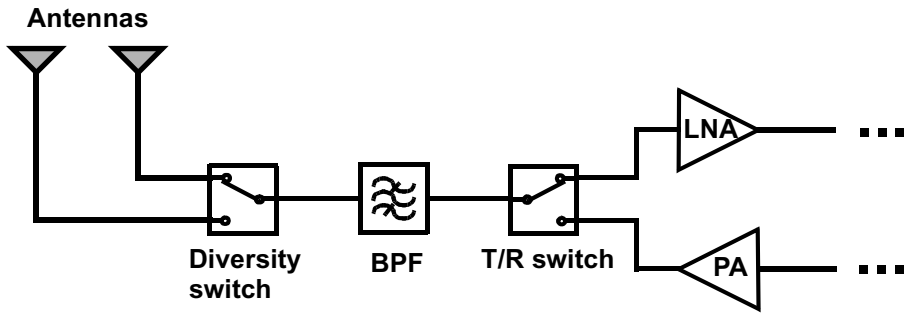


Figure 3-1 WLAN transceiver with two antennas in single band implementation

inputs to outputs when switches are on and off, respectively. Return loss represents how much power is reflected back from input/output, and it is determined by input/output impedance. Insertion loss and isolation can be obtained by measuring S_{21} when switches are on and off, respectively. When the input port characteristic impedance (Z_{o1}) is equal to the output port characteristic impedance (Z_{o2}), the insertion loss or the isolation in dB can be calculated as -20log(S_{21}). Return losses in dB are -20log(S_{11}) and -20log(S_{22}). P_{1dB} interprets the switch power handling capability, and it also characterizes the linearity of a switch along with IP_3. The linearity requirements are much higher in the transmitter than those for the receiver. For WLAN applications, outputs of a switch have to satisfy output spectrum masks defined in the IEEE standards (see Chapter 1).

Today, most RF switch modules are implemented in GaAs technology. Because of this, the switches can not be integrated with the other RF components. CMOS technology has the potential to integrate all digital and analog circuits into a single chip. This has been the motivation to find ways to implement RF switches in a bulk CMOS technology.

Compared to GaAs transistors, CMOS transistors suffer from lower mobility which is critical for RF switch design. The electron mobilities are 9200 cm^2/V-s and 1450 cm^2/V-s for GaAs and Si at 300 ^oK, respectively [18]. So, the minimum channel sheet resistance (ρ_{ch}) is about 2000 Ω/square for an NMOS transistor [19] given the maximum electric field less than 5 MV/cm across the gate oxide layer. The channel resistance (R_{ch}) is directly related to the switch insertion loss [20]. The insertion loss decreases with lower channel resistance. The channel resistance (R_{ch}) is $\rho_{ch} \cdot W/L$, here W and L are MOSFET channel width and length, respectively. The channel width can not be arbitrarily increased due to a corresponding increase of the drain/source parasitic capacitance. A silicon sub-

strate is lossy. Without careful design, the parasitic capacitor and resistor associating with it will introduce a significant loss and limit CMOS switch isolation. Combatting the substrate loss is another consideration in RF CMOS switch design. To achieve better insertion loss using CMOS technology, channel length, *L* must be scaled. Since the parasitic capacitance is also reduced with scaling, the insertion loss improves [20]. But technology scaling reduces power supply voltage in order to keep the maximum electric field across the gate oxide in a safe range. This in turn lowers the switch power handling capability. A large output power requires a large voltage swing across an output load (50 Ω). To make this even worse, an additional reliability issue has to be evaluated for CMOS switch design due to the presence of a gate oxide layer. All these make implementation of CMOS RF switches challenging.

Both 5-to-6-GHz and 2.4-GHz CMOS switches are included in the proposed multi-band receiver. For frequencies higher than 5 GHz, CMOS may not be adequate due to its inherently lossy substrate and lower mobility. A 5.8-GHz CMOS switch fabricated in a 0.18 μm CMOS technology is described in section 3.2. For the first time, a bulk CMOS switch which can operate up to the 6-GHz band is demonstrated. A 2.4-GHz switch with improved power handling capability is discussed in section 3.3. This 2.4-GHz switch incorporates a voltage doubler and a control circuitry and requires a single 3-V supply.

3.2 5.8-GHz 0.18μm CMOS Switches

3.2.1 Design of 5.8-GHz CMOS Switches

The previous works have shown that the insertion loss can be minimized by either making the substrate resistances sufficiently high or sufficiently low [20,21,22]. The over-

all limits of substrate resistances are the p-well doping, substrate resistivity and layout. A low substrate resistance layout is favored when a p^+ substrate is used, since the maximum attainable substrate resistances are inadequate to achieve sufficiently low insertion loss, whereas sufficiently high substrate resistances may be achieved for acceptable insertion loss, when a p^- substrate is used. In order to examine the potential of 0.18-μm CMOS switches for 5 – 6 GHz wireless LAN applications as well as the effects of substrate resistances, two 0.18-μm CMOS switches were fabricated utilizing 20-Ω-cm p^- substrates: the high substrate resistance switch (HSRSW) and the low substrate resistance switch (LSRSW) with near the maximum and minimum substrate resistances that can be obtained in the process, respectively [23].

As shown in Figure 3-2, the schematic of SPDT RF T/R switch is similar to the previously reported 900-MHz and 2.4-GHz switches [21,22]. In Figure 3-2, the capacitors except C_{B1} and C_{B2} are parasitic capacitors of transistors and R_B's are substrate resis-

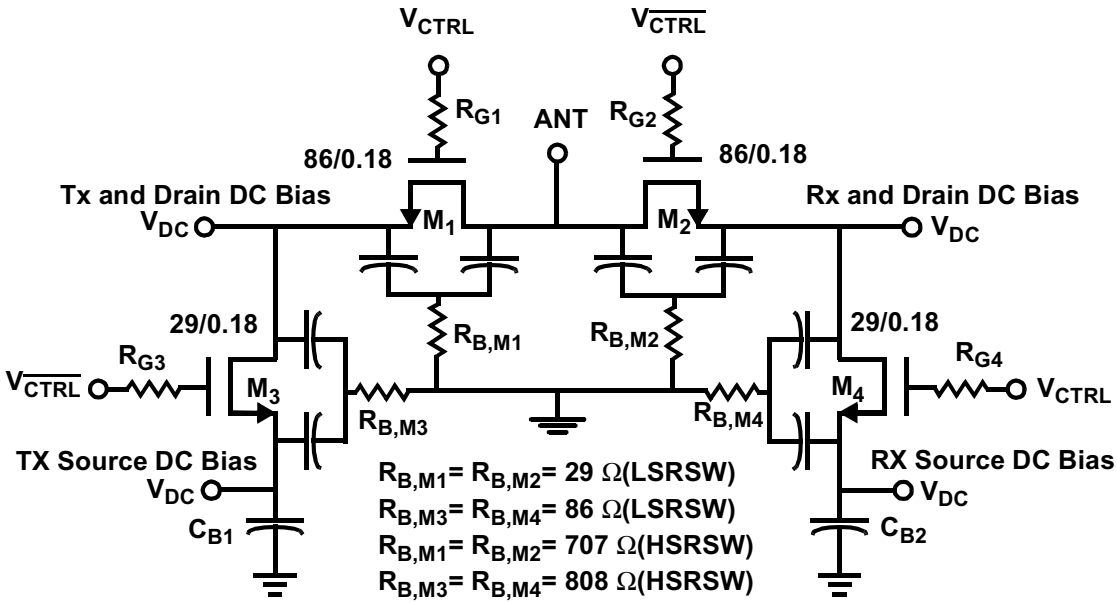
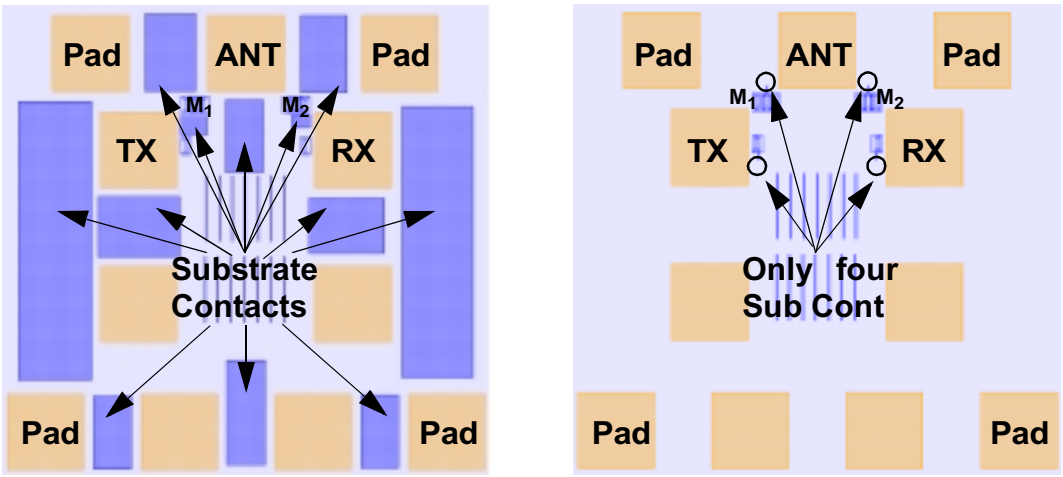


Figure 3-2 A 5.8-GHz switches schematic with low and high substrate resistance



(a) (b)

Figure 3-3 5.8 GHz switch layouts, only show pads and substrate contacts (a) LSRSW (b) HSRSW

tances. C_{B1} and C_{B2} are by-pass capacitors to ac ground the sources of M_3 and M_4. The transistor sizes are also listed in the figure.

The effects of substrate resistances on CMOS switch were explained in Huang [20]. In this implementation, HSRSW utilizes only one minimum size substrate contact (0.44µm x 0.44µm) for each transistor to achieve as high substrate resistances as possible. On the other hand, a large number of substrate contacts was used in LSRSW to minimize substrate resistances. The Figure 3-3 shows the substrate contacts in LSRSW and HSRSW. The majority of the LSRSW area is occupied by substrate contacts. On the contrary, HSRSW only has four minimum size substrate contacts. Figure 3-2 also includes a list of measured values of the key substrate resistances. For $R_{B,M1} = R_{B,M2}$, the measured substrate resistances are 29.3 Ω and 707 Ω for LSRSW and HSRSW, respectively. For $R_{B,M3} = R_{B,M4}$, the measured substrate resistances are 85.6 Ω and 808 Ω for LSRSW and HSRSW, respectively. The resistances are measured using test circuits identical to the

switches except that the drain/source-to-body junctions are replaced with p^+ substrate contacts [24].

The substrate resistances also affect the isolation. The low substrate resistances provide a low impedance path between the signal and ground leading to better isolation. The switch power handling capability (P_{1dB}) depends on the dc bias of TX and RX nodes. The P_{1dB} can be limited by potentially three effects: 1. input signal is so large that the drain/source-to-body junctions of M_1/M_2 are forward biased; 2. M_3 or M_4 is unintentionally turned on and input signal has a path to ground; 3. and the voltage across gate oxide is too large to guarantee its long term TDDB reliability [25]. For a given dc bias V_{DC}, the effects 2 and 3 set conflicting requirements for V_{CTRL}/$V_{\overline{CTRL}}$. Without losing generality, if the Tx to antenna path is assumed to be on, i.e., V_{CTRL} is high, then the effect 2 requires lower $V_{\overline{CTRL}}$ to keep M_2 and M_3 turned off at all time, but effect 3 needs $V_{\overline{CTRL}}$ sufficiently high to limit the voltage across the gate oxide.

The dc bias conditions are evaluated using Cadence SpecterS simulations. When V_{DC} and V_{CTRL} are set to 1.8 and 3.6V, respectively, the relationship between $V_{\overline{CTRL}}$ and P_{1dB} is shown in Figure 3-4. The V_{gd} is the gate to drain voltage of M_2 or M_3. It is the maximum voltage between transistor gate and drain/source during the switch operation. Input P_{1dB} (IP_{1dB}) is affected by effect 2. As $V_{\overline{CTRL}}$ increases, M_3 or M_4 is easier to be turned on and IP_{1dB} drops. During the switch operation, the peak voltages across gate oxide should never exceed the safety limit for the TDDB reliability of 2.5 V [25]. From Figure 3-4, the $V_{\overline{CTRL}}$ has to be larger than 1.3V to ensure $|V_{gd}| \le 2.5V$.

Figure 3-5 shows the micro-photograph of the 5.8 GHz CMOS switches. All components including the transistors, resistors (R_g's) and capacitors (C_{B1} and C_{B2}) shown in

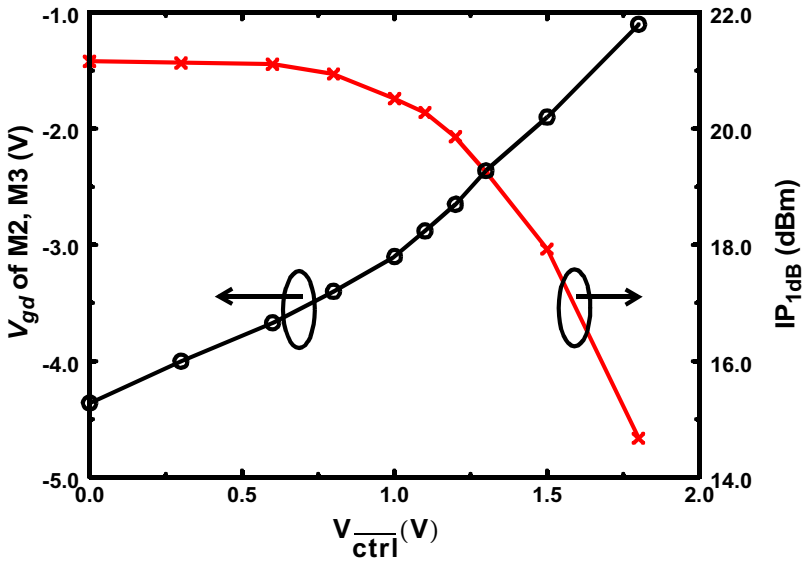
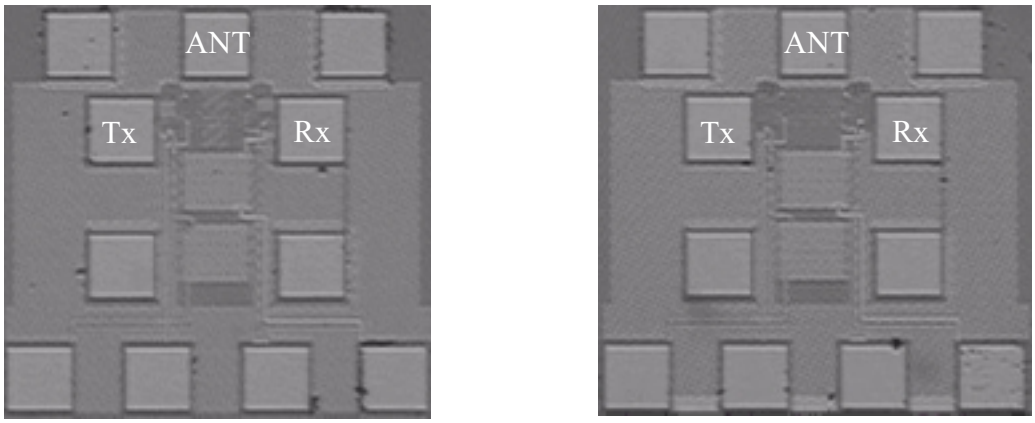


Figure 3-4 Cadence Spectres simulations show the relationship between $V_{\overline{CTRL}}$ and V_{gd}, and $V_{\overline{CTRL}}$ and IP_{1dB}

Figure 3-2 are integrated. The chip area is the same for LSRSW and HSRSW, and 473x451 μm^2.

3.2.2 Experimental Results of the 5.8-GHz CMOS Switches

The switch measurements are performed on wafer. Figure 3-6 shows the measured insertion loss and isolation. The insertion loss is about 0.8 dB for LSRSW and is 1.0 dB for HSRSW, and the isolation is more than 29 dB for LSRSW and is 27 dB for HSRSW,



(a) (b)

Figure 3-5 A micro-photograph of (a) the LSRSW, and (b) the HSRSW.

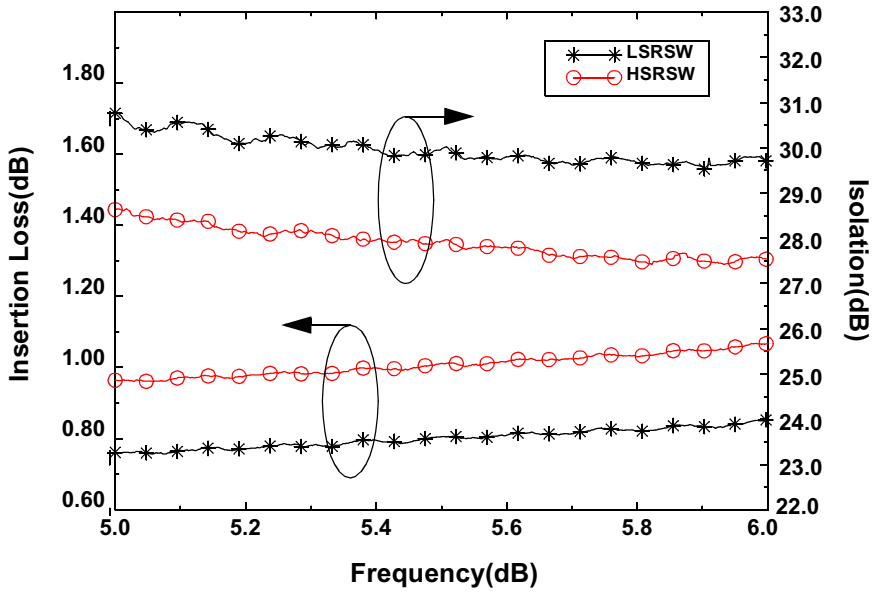


Figure 3-6 Measured insertion loss and isolation for HSRSW and LSRSW

both at the same operating frequency of 5.825GHz, and at V_{CTRL} or V_{GB}=3.6 V, $V_{\overline{CTRL}}$=1.3V and drain/source-to-body reverse bias (V_{DB} and V_{SB}) of 1.8 V. The retune loss is better than 12dB between 5 and 6 GHz for both switches. Figure 3-7 shows the measured return loss for LSRSW.

The power measurement results of the switches at 5.825 GHz are shown in Figure 3-8. When V_{CTRL}= 3.6 V and $V_{\overline{CTRL}}$ = 1.3V, TX and ANT nodes are connected. Output P_{1dB} is 18 dBm for HSRSW and 17 dBm for LSRSW. These are excellent results considering the voltage limitations of the 0.18-μm CMOS process. Output third order intercept point (IP_3) was measured using a two-tone test. IP_3's for both switches are around 33 dBm.

The overall switch characteristics are summarized in Table 3-1. LSRSW is the first bulk CMOS switch to have an insertion loss less than 1 dB up to 6 GHz. The reliability test is also performed. With ANT node open, which represents infinite VSWR, switches

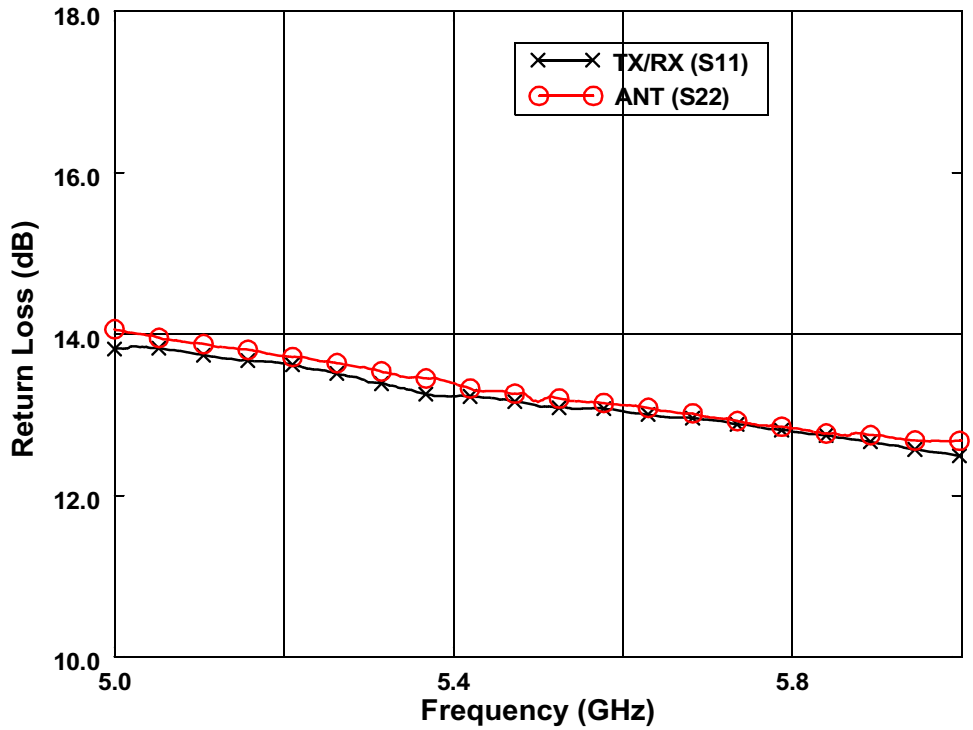


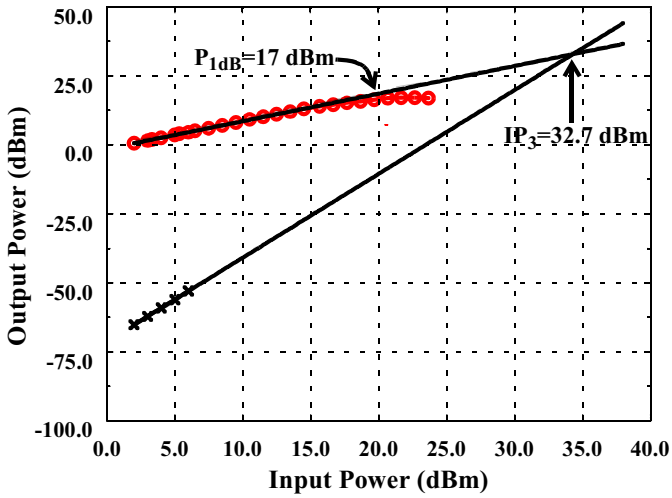
Figure 3-7 Measured LSRSW input and output retune loss at 5.825 GHz when switches are on.

were stressed for one hour at input power of 17 dBm for LSRSW and of 18 dBm for HSRSW, respectively. No degradation was observed on insertion loss and isolation after the stress.

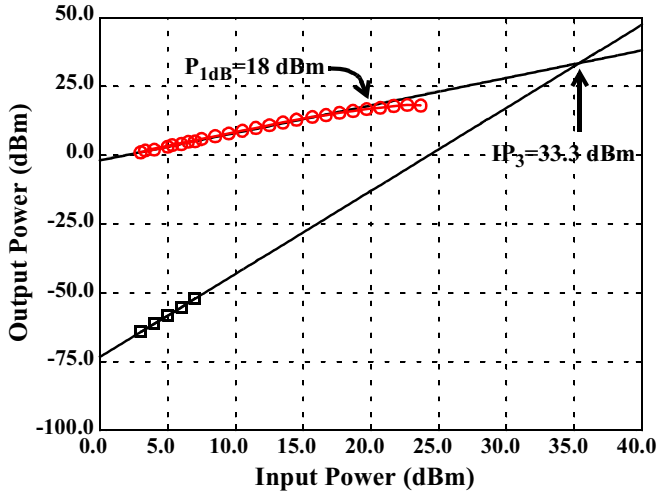
Besides the higher insertion loss for HSRSW, another difficulty for HSRSW is when the switch is integrated with the other circuits, for example, a low noise amplifier (LNA) or a power amplifier (PA), the substrate contacts of the LNA and PA will reduce

Table 3-1 Summary of Switch Performances at 5.825GHz

Switch	LSRSW	HSRSW
Insertion Loss (dB)	0.8	1
Isolation (dB)	29.6	27.5
Return Loss (dB): S_{11}/S_{22}	12.7/12.8	14.8/14.4
P_{1dB} (dBm)	17	18
IP_3 (dBm)	32.7	33.3



(a)



(b)

Figure 3-8 The output 1dB compression point and IP_3 measurements of (a) LSRSW and (b) HSRSW at 5.825GHz

HSRSW substrate resistances, degrading switch performance, while this will slightly improve the performance of LSRSW. Because of these, low substrate resistance layouts are preferred for RF switches in the 0.18-μm CMOS process [23].

3.2.3 Discussions on 5.8-GHz CMOS Switches

Two single-pole, double-throw transmit/receive switches were designed and fabricated with different substrate resistances using a 0.18-μm p^- substrate CMOS process. The switch with low substrate resistances exhibits 0.8 dB insertion loss and 17 dBm P_{1dB} at

5.825GHz, whereas the switch with high substrate resistances has 1-dB insertion loss and 18-dBm P_{1dB}. These results suggest that the optimal insertion loss can be achieved with low substrate resistances and 5.8-GHz T/R switches with excellent insertion loss can be implemented in a 0.18-μm CMOS process.

For IEEE 802.11 wireless LAN applications, the power handling capabilities of these switches are not sufficient. An IEEE 802.11a compliant transmitter with 17.8 dBm output power has been reported [26]. At this input power level, HSRSW insertion loss is almost 1.8 dB, which is somewhat high. Also, the input power level to T/R switches has to be back off several dB from IP_{1dB} point from the linearity point of view. The T/R switch input P_{1dB} has to be significantly larger than 20 dBm for WLAN 802.11a applications. There are several solutions to deal with the CMOS switch power handling capability. One way to solve this problem is to put the transmitter switch before the power amplifier (PA). If both the PA driver, PA and switches are integrated in one single chip, it should be easy to insert a switch between the PA and PA driver. This will greatly reduce the P_{1dB} requirement for the switches. If the PA employes a differential topology, the P_{1dB} requirement of the switch could be lowered by another 3 dB. Another way to improve CMOS switch power handing capability is to use circuit techniques to enhance P_{1dB}. Among them, there are impedance transformation [20,27,28], LC-tuned substrate bias [29] and stacked depletion-layer-extended transistors [30].

If the aggregate loss from a T/R switch, a BPF and the board is assumed to be 3 – 4 dB, the output power reaching the diversity switch could be less than 15 dBm. For this power level, LSRSW/HSRSW can be integrated and used as diversity switches.

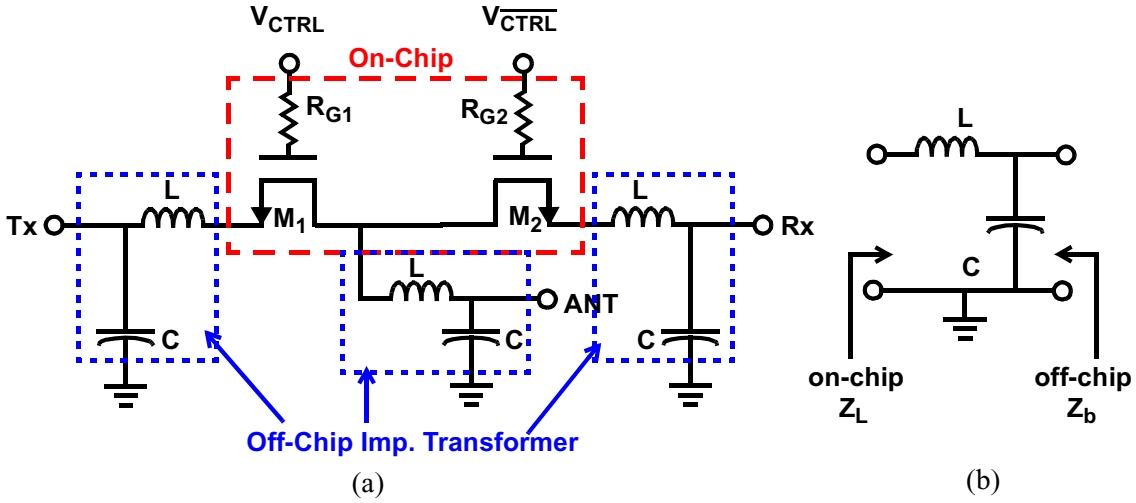


Figure 3-9 A 2.4-GHz CMOS switch. (a) A schematic, (b) Off-chip impedance transformer.

3.3 2.4-GHz 0.25µm Switches with Impedance Transformers

3.3.1 Design of 2.4-GHz Switches with Impedance Transformers

One way to boost switch power handling capability is to use impedance transformation [20,27,28]. A 2.4-GHz CMOS switch reported by O and Huang [27] has 1.1dB insertion loss and 20.6 dBm P_{1dB}, which is adequate for WLAN applications. However, a 6-V bias is used [27]. It is much higher than the normal power supply range (2.7 – 3.6 V) for WLAN products. The switch presented in this section incorporates a voltage doubler and control logic circuitry, thus works with only single power supply and one-bit control signal. The 21-dBm P_{1dB} has been achieved with impedance transformation. The circuit was fabricated in a 0.25-µm foundry CMOS process.

The switch schematic is shown in Figure 3-9(a). Compared to the 2.4-GHz switch of [27] and the 5.8-GHz CMOS switch, the two shunt transistors (M_3, M_4 in Figure 3-2) are omitted. The switch core only contains two transistors, M_1 for the transmitter chain and M_2 for the receiver. M_1 and M_2 are identical with a size of 500µm/0.24µm. V_{CTRL}

and $V_{\overline{CTRL}}$ are complementary control signals, and are applied to gates of M_1 and M_2 through two on-chip ploysilicon resistors $R_{G1}$and R_{G2}, respectively.

In order to improve the switch power handling capability, impedance transformation is used to reduce the impedance seen by the transistors [20]. The impedance transformation is realized using a series L-shunt C matching network as shown in Figures 3-9(a) and (b). The impedance Z_b should be ~50 Ω for matching to the off-chip transmission line. The impedance Z_L which is seen by the transistors are transformed down to ~ 25 Ω. Assuming the passive matching network is lossless, the total power delivered to the load is increased because $Power=|V_{out}^2/Re(Z_L)|$. The total voltage swing V_{out} is limited by the transistor operation voltage, and the power handling capability increases as the output load impedance Z_L decreases. The series L is formed using a bondwire, and shunt C is an off chip component. When the load impedance Z_L seen by the transistor is reduced, the transistor channel on-resistance to load impedance ratio increases [20] and the switch insertion loss increases. There is a trade-off between switch insertion loss and P_{1dB}. WLAN applications could tolerate worse insertion loss than reported in [22]. The impedance transformation provides a mean to balance insertion loss and P_{1dB} to optimize the overall performance.

The drains and sources of the switch transistors are biased at 3 V to increase P_{1dB} and lower insertion loss [21]. Since in the 0.25-μm CMOS process, the nominal transistor operation voltage is 2.5 V, the switch requires higher than 5V control voltage for proper operation. A voltage doubler and switch control logic circuits operating at 5.5 V are integrated on the same chip to enable operation using a single 3 V supply voltage [28]. the voltage doubler is a charge pump cell type doubler with improved PMOS series switches

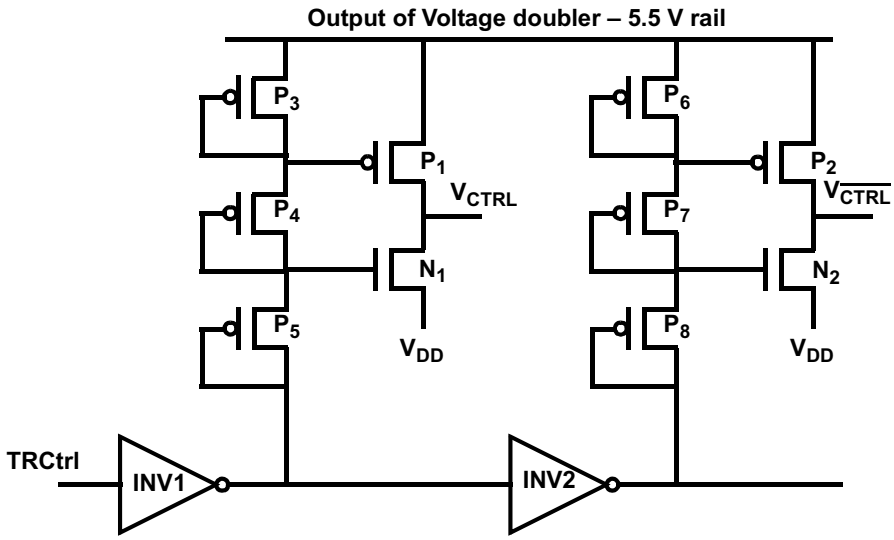


Figure 3-10 A schematic of control logic circuit

[31]. The 22-MHz a reference clock signal for the phase-lock loop (PLL) is used as the input signals for the voltage doubler. The measured voltage doubler outputs versus power supply is given in Table 3-2. The voltage doubler schematic is the same as that of Favrat [31].

The output of voltage doubler is fed into the control logic circuit. A schematic of the control logic circuit is shown in Figure 3-10. TRCtrl is an one-bit control signal from the baseband DSP circuit and goes through two on-chip inverters INV1 and INV2 to control output. P_1 and N_1, and P_2 and N_2 pair form two inverters which drive V_{CTRL} and $V_{\overline{CTRL}}$ node and operate between V_{DD} and the voltage doubler output, 5.5 V. One of the outputs of INV1 and INV2 is grounded. But since there are three transistors, P_3, P_4, P_5 or P_6, P_7, P_8, inserted between the ground and 5.5 V, V_{gs}'s and V_{ds}'s in the logic circuit are kept less than 2.5 V. To provide greater safety margin, the circuit is implemented using the

Table 3-2 Measured voltage doubler output versus power supply voltage

Power Supply (V)	2.7	3	3.3	3.6
Doubler Output (V)	4.9	5.4	5.8	6.2

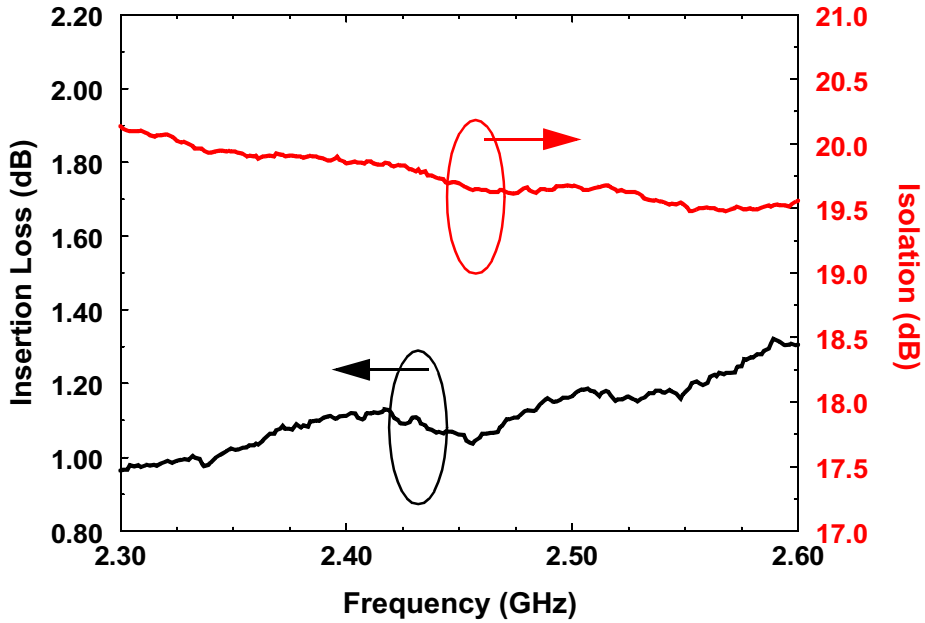


Figure 3-11 Measure switch insertion loss and isolation when V_{DD} is 3 V

thick oxide 3.3-V I/O transistors in the 0.25μm process. When TRCtrl is high, V_{CTRL} is high and $V_{\overline{CTRL}}$ is low; and when TRCtrl is low, V_{CTRL} is low and $V_{\overline{CTRL}}$ is high.

3.3.2 2.4-GHz Experimental Results

The insertion loss and isolation of switch versus frequency plots are shown in Figure 3-11. At V_{DD} = 3 V, the measured insertion loss for the switch is 1.1 to 1.2 dB and isolation is 19.8 dB at frequencies between 2.4 and 2.5 GHz. The low insertion loss and reasonable isolation are realized by lowering substrate resistances [21]. The output power versus input power plot measured at 2.4GHz for the switch is shown in Figure 3-12. Input P_{1dB} (IP_{1dB}) of the switch is 23.1 dBm while P_{1dB} is 21 dBm. The P_{1dB} is improved 3.2 dB over Huang [22] while insertion loss is still reasonable. A good balance between insertion loss and P_{1dB} is achieved by using impedance transformation. The switch return loss is better than 15 dB for the measurement frequency range between 2.3 to 2.6 GHz.

Table 3-3 Measured insertion loss, isolation and P_{1dB} versus power supply

Power Supply (V)	Insertion Loss (dB)	Isolation (dB)	Input P_{1dB} (dBm)
2.7	1.07	22.7	22.8
3	1.05	22.6	23.2
3.3	1.02	22.4	23.8
3.6	1.01	22.4	24.5

Since the switch, voltage doubler and control logic circuit work together, the switch insertion loss and P_{1dB} improve as power supply voltage increases. Table 3-3 shows the measured insertion loss, isolation and P_{1dB} for V_{DD} from 2.7 to 3.6 V. These data were measured using a different die, so data are slightly different. The P_{1dB} is 22.5 dBm at V_{DD} = 3.6 V. At this condition, the voltage doubler output is 6.2 V.

FCC requires that power emission at the 2nd and 3rd harmonic frequencies must be less than -41.25 dBm/ MHz. The T/R switch output is bandpass filtered and the high order harmonics are suppressed. This switch can also potentially be used as an antenna diversity switch. Since, for this application, there is no filter following the switch except

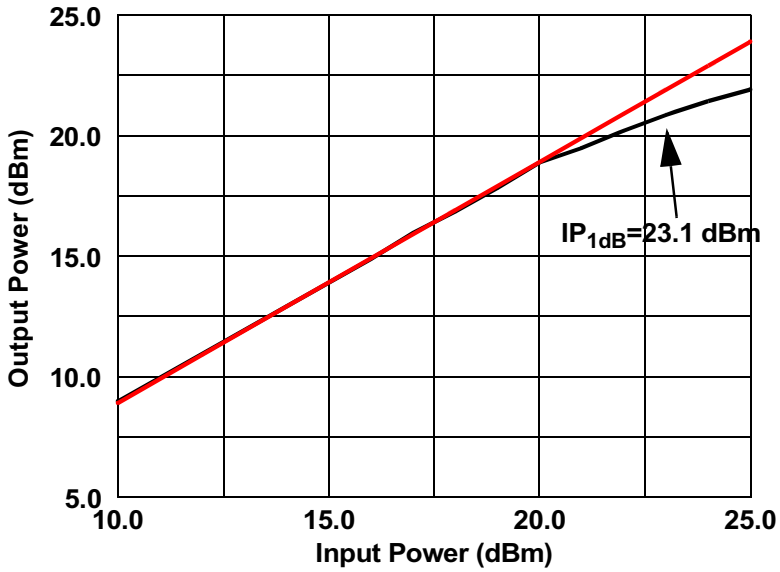


Figure 3-12 Measured switch 1dB compression point at 2.4 GHz

Table 3-4 Switch harmonic response at 11 Mbps QPSK input signal

2.4GHz input power(dBm)	2.4GHz output power(dBm)	4.8 GHz 2nd harmonic(dBm/MHz)	7.2 GHz 3rd harmonic(dBm/MHz)
20	18.88	-49.5	-51.5
21	19.47	-46.5	-47.4
22	20.2	-44.8	-44.8

for the frequency response of antennas, harmonic response of the switch is critical. Harmonic response of the switch has been characterized by applying a DSSS QPSK signal with a 11 Mbps data rate. Table 3-4 shows the measured results with three different input power levels. Even at input power of 22 dBm, the output power levels of the 2nd and 3rd harmonics are less than -44 dBm/MHz without including the filtering effects of the antennas. The harmonics whose orders are higher than 3 have much lower power and will not violate the FCC rules. These results indicates that this switch can be integrated with the power amplifier without radiating excessive harmonic power.

The switch circuit with a voltage doubler and a control logic circuit was measured with a transmitter chain [28]. The 802.11b compliant output mask was obtained at the switch output. Figure 3-13 shows the output spectrum for the entire transmitter chain including the switch under the modulation with a DSSS 11 Mbps QPSK signal. The output power level is 16.5 dBm. As shown in the figure, it satisfies the spectral mask requirement for 802.11b. At this power level, the spurs due to the 22-MHz reference expected from the voltage doubler is not detected in the transmitter output. The switch is acceptable for WLAN applications.

To evaluate the reliability, the switch has been stressed at a PA output power level of +23.0 dBm for more than 3 months. No apparent shifts in the switch characteristics

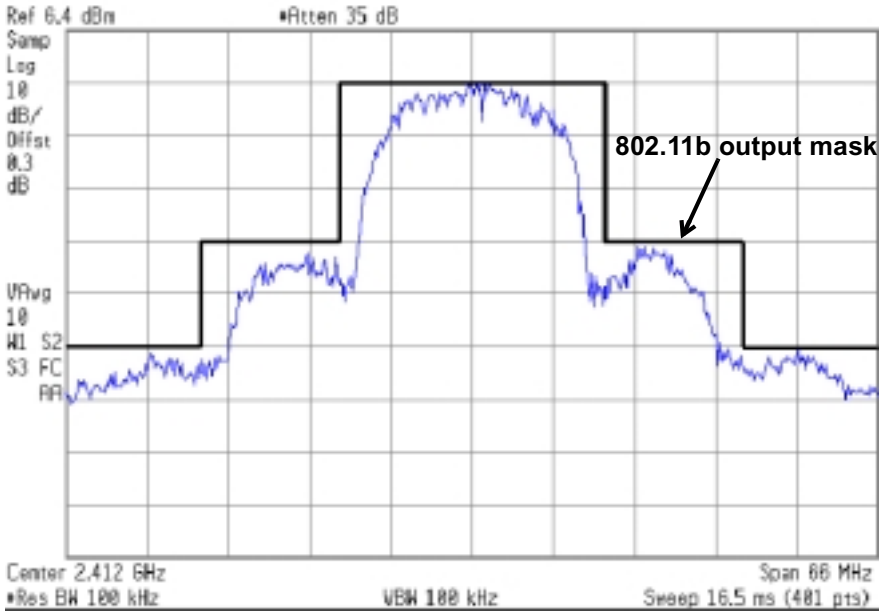


Figure 3-13 Measured transmitter output spectrum, it satisfies 802.11b spectral mask requirement.

have been observed. The switch has also been stressed by mismatching the output to 20:1 VSWR. The switch survived the stress at 20-dBm output power.

The die photograph of the switch is shown in Figure 3-14. The voltage doubler and logic control circuits are not placed close to the switch, and not shown in the photograph.

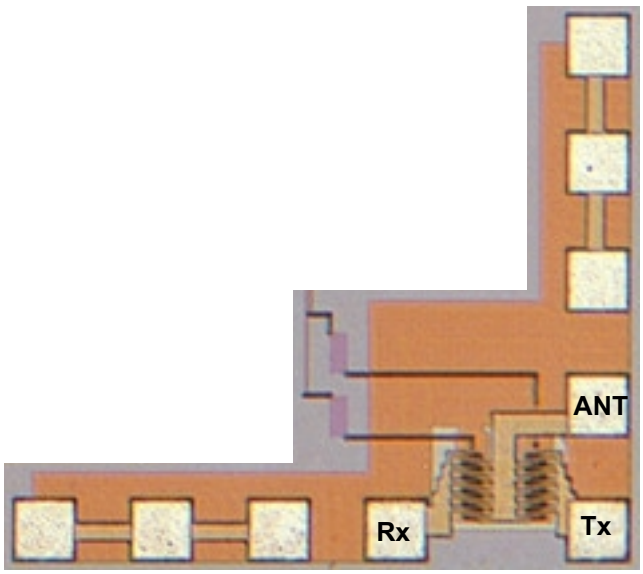


Figure 3-14 A micro-photograph of 2.4-GHz switch. The voltage doubler and logic control circuit are not shown.

3.3.3 Conclusion

A 2.4-GHz CMOS switch fabricated in a 0.25-μm CMOS technology exhibits 1.1-dB insertion loss and 23.1-dBm input P_{1dB}, which are sufficient for WLAN applications. A voltage doubler and a logic control circuit are integrated with this switch to operate with a single 3-V power supply. The measurements with a power amplifier show that the combination is 802.11b compliant. The switch also survived stringent reliability tests. All measurement results suggest that for 2.4-GHz WLAN applications, CMOS T/R switch can be integrated with other of circuits. This switch can be used as either a T/R switch or a diversity switch shown in Figure 3-1. The measured output harmonic power is also compliant to the FCC regulations.

A 5.825-GHz CMOS switch fabricated in a 0.18-μm CMOS technology exhibits 0.8-dB insertion loss and 17-dBm input P_{1dB}. For IEEE 802.11a wireless LAN application, the power handling capabilities of these switches are not sufficient for use as a T/R switch. CMOS switch P_{1dB} at high frequencies needs to be improved, and the results from such a effort to achieve this is be described in the Chapter 4.

CHAPTER 4
15-GHZ FULLY INTEGRATED CMOS SWITCHES

4.1 Introduction

As stated in Chapter 3, CMOS switch power handling capability at high frequencies is an area needed to be investigated. In this chapter, two 15-GHz CMOS RF switches have been fabricated and characterized, to demonstrate a technique to improve CMOS switch P_{1dB} at high frequencies. Though, a 15-GHz CMOS switch is not directly related to the proposed multi-band receiver, this study serves two purposes: first, it explores a technique to increase CMOS switch power handling capability, which is one of the design issues of multi-band receiver; second, it breaks the previous CMOS switch operation frequency record, increasing it from 6 to 15 GHz. This indeed widens the applications of CMOS technology, which is congruous with the theme of this dissertation.

The first switch is designed with on-chip LC impedance transformation networks (ITN's). The second switch without ITN's is also implemented and used for comparison. Integrating ITN's improves P_{1dB} by 6.5 dB without any sacrifice of the insertion loss. But its frequency response is no longer broadband, i.e., it has tuned response. The switch without ITN's has good insertion loss from DC up to 15 GH but with lower P_{1dB}, which is described in section 4.2. The switch with ITN's is illustrated in section 4.3. It shows that the degradation of insertion loss due to use of ITN's can be compensated by reducing the increase of insertion loss due to the bond pad capacitances in the switch without ITN's. The comparison of two switches' performances clearly demonstrated the design trade-offs

of integrated ITN's. Both CMOS switches do not have as high isolation as the commercial GaAs switch [32]. The switch isolation model is analyzed in section 4.4 and conclusions are given in section 4.5.

4.2 15-GHz CMOS Switch with a Typical Topology

As stated in Chapter 3, CMOS switch design at high frequencies is a challenge. In order to achieve low insertion loss, a 0.13-μm CMOS technology with copper interconnection is chosen for 15-GHz switch design. The first CMOS switch is implemented by using a typical CMOS switch topology [21-23, 32]. The switch schematic is shown in Figure 4-1.

Two transistors (M_1 and M_2) in series to form a single-pole-double-throw switch. M_3 and M_4 are two shunt transistor to improve the switch isolation. C_{B1} and C_{B2} are on-chip 10-pF bypass capacitors for ac-grounding sources of M_3 and M_4. All on-chip resistors are for DC bias and AC isolation. Rx, Tx and ANT nodes as well as sources of

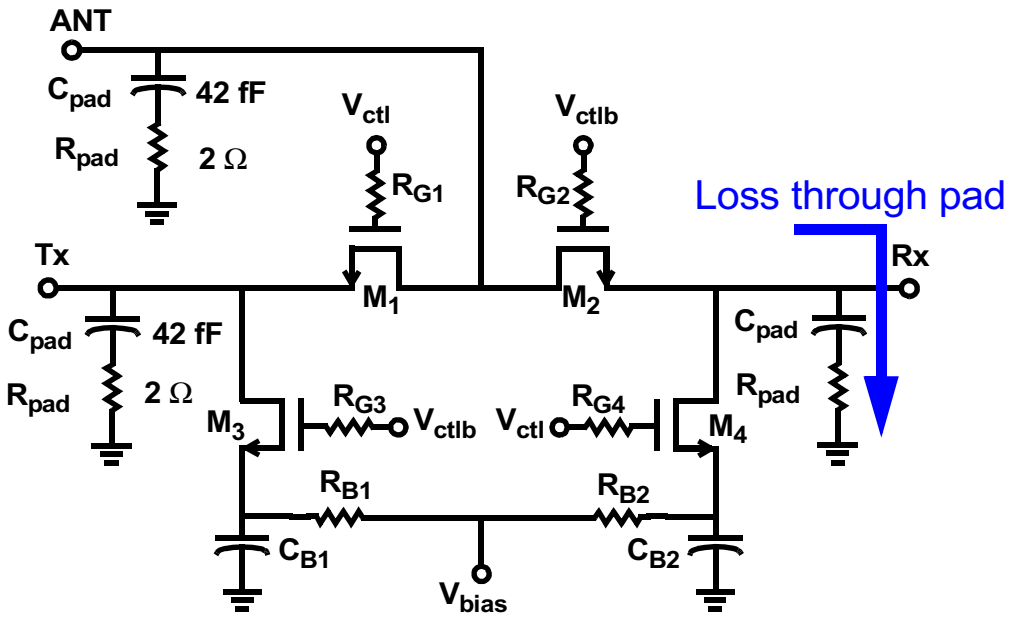


Figure 4-1 A schematic of 15-GHz CMOS switch, with a typical integrated switch topology.

M_3 and M_4 are DC-biased at 1.8 V. This voltage reverse bias the drain/source to substrate p-n junctions, improve power handling capability, reduce insertion loss and increase isolation [21-23]. V_{ctl} and V_{ctlb} are control voltages and set to either 3.0 V (on) or 1.2 V (off). Because of this, the voltage across the gate oxide never exceeds 1.2 V.

The parasitics of input/output pads are also included in this switch schematic. The circuit model of pads is represented by a 42 fF capacitor (C_{pad} in Figure 4-1) in series with a 2 Ω resistor (R_{pad} in Figure 4-1). This pad model is extracted from the measurements of an open test structure. The pad is shielded by silicided p^+ diffusion to improve its quality factor (Q). With finite channel resistance of transistors, the pad capacitance introduce losses to the switch. At low frequencies, this loss is usually negligible. But at the high frequencies, this loss could be a significant part of total switch insertion loss.

The switch insertion loss is illustrated in Figure 4-2. It shows both measured and simulated data. At 15-GHz, it achieves 1.8-dB measured insertion loss, which is excellent and comparable with that of the GaAs switch [32]. The simulated switch insertion loss with pad impedance agrees with the measured data at low frequency, but at high frequency, the discrepancy is larger. This may due to the inaccuracy of MOS transistor model at high frequencies. At 15-GHz, the discrepancy is about 0.15 dB, which is small. For comparison, the switch insertion loss is also simulated without the pad impedance. The insertion loss difference with and without the pad is 0.5 dB at 15 GHz. The presence of pad degrades the switch insertion loss by 35% at this frequency point. So, the pad loss must be carefully considered for high frequency CMOS switch design. The switch designed without including the pad impedance also will benefit to the insertion loss, as we

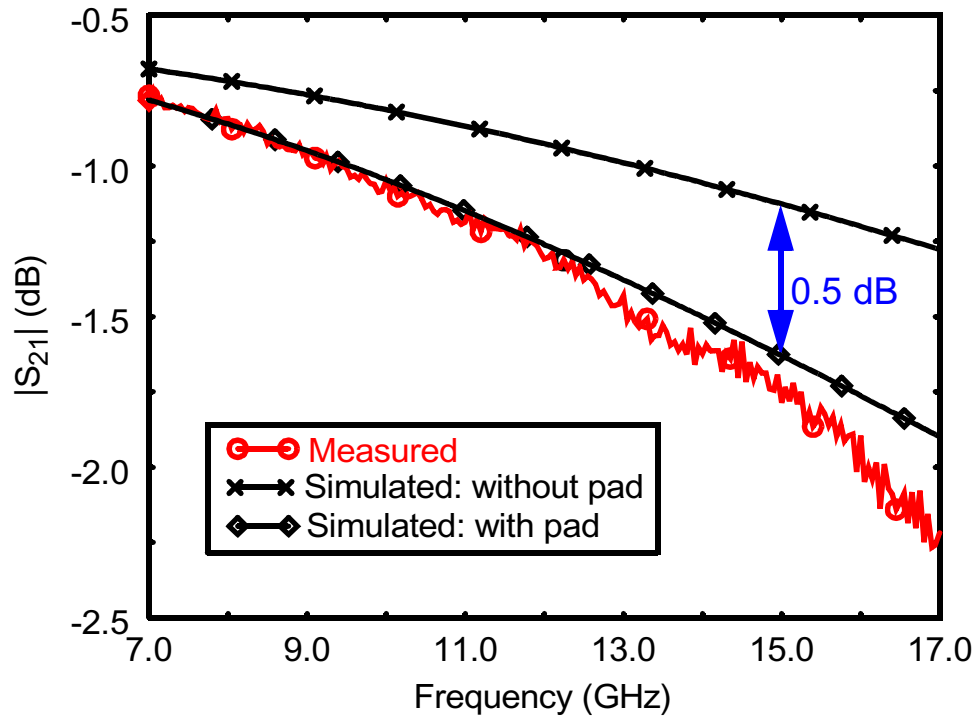


Figure 4-2 The 15-GHz CMOS switch insertion loss, shows both measured and simulated data.

will see it in the next section of CMOS switch with the integrated impedance transformation networks.

This switch has very broad frequency response. As shown in Figure 4-3, the switch also has been measured from 2 to 12 GHz. $|S_{11}|$ is measured at the ANT node and $|S_{22}|$ is measured at either Tx or Rx node. The switch has good input and output return losses (better than 10 dB) up to 10.65 GHz. The parasitic capacitance which is shunted to ground impairs the return losses and deviate them away from ideal at high frequencies. The measured insertion loss is 0.6 and 1.1 dB for 2 and 10.6 GHz, respectively. The measured isolation is higher than 23 dB from 2 to 12 GHz.

The switching time is specified by t_{on}, t_{off} and t_{rise}, t_{fall}. t_{on} and t_{rise} represent the switch turn-on time; t_{off} and f_{fall} the turn-off time. t_{on} and t_{off} is defined as the difference

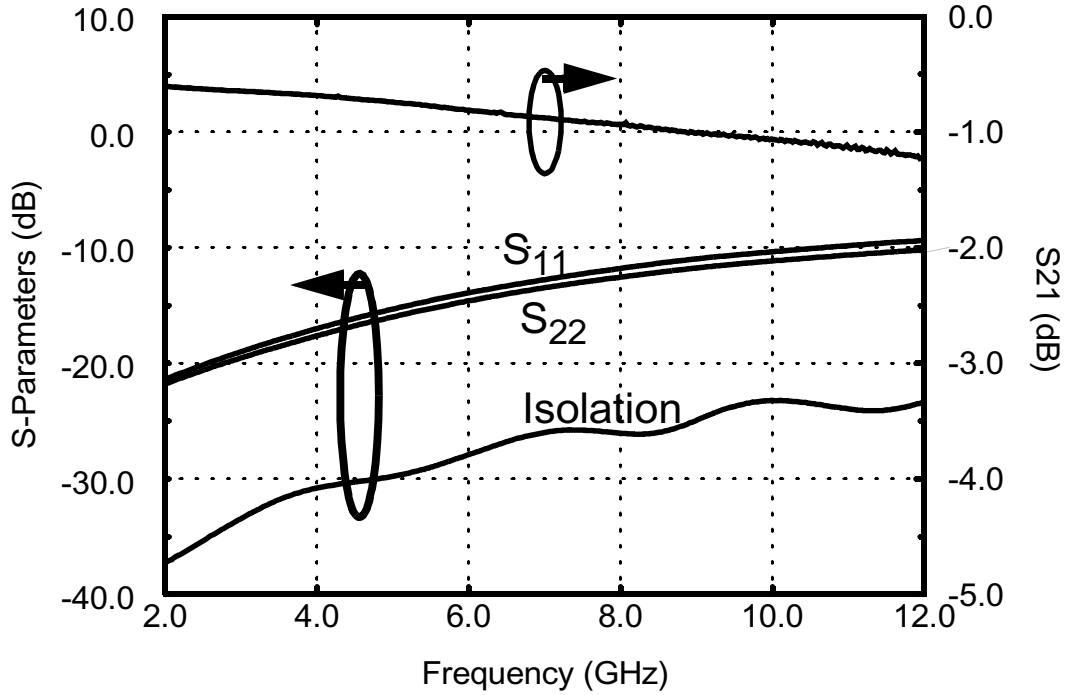


Figure 4-3 Measured insertion loss, isolation and return losses for 15-GHz CMOS switch with a typical switch topology.

between the time for 50% control voltage and the time for 90 and 10% of RF signal amplitude, respectively. t_{rise} is defined as difference between the time at 10% and time at 90% of RF signal amplitude. Similarly, t_{fall} is defined as the difference between the time at 90 and the time at 10% of RF signal amplitude. The simulated t_{on}, t_{off}, t_{fall} and t_{rise} are 0.5, 0.25, 0.25 and 0.1 ns, respectively.

The measured switch input P_{1dB} is 15 dBm. This is 10-dB lower than that of the GaAs switch [32]. Is there any way to improve the CMOS switch P_{1dB} while the switch insertion loss is still kept an acceptable level? A technique to accomplish this is discussed in section 4.3.

Though this switch does not achieve high P_{1dB} due to the low transistor operation voltage (1.2 V), it clearly shows a broadband operating frequency range. Its performance over 2 to 10.6 GHz frequency band should be sufficient for the ultra wide band (UWB)

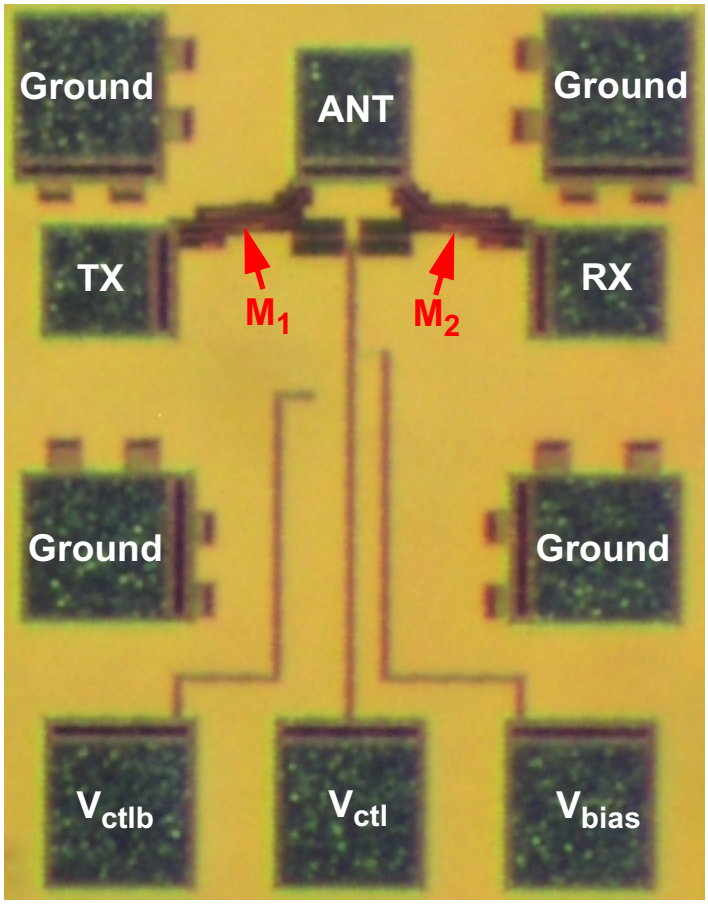


Figure 4-4 The die photo of the 15-GHz CMOS switch, which is designed with a typical integrated switch circuit topology.

applications. UWB requires a low transmitter power but large bandwidth from 3.1 to 10.6 GHz. This switch is the first CMOS switch that has sufficient performance for UWB applications. This is also the first CMOS switch that has excellent insertion loss from DC to 15 GHz.

The die photo of the switch is shown in Figure 4-4. The chip area is 0.4 x 0.5 mm^2.

4.3 15-GHz CMOS Switch with ITN

4.3.1 Integrated LC Impedance Transformation Network(ITN)

The impedance transformation networks (ITN's) have been used to improve CMOS switch power handling capability [23,27,33]. But, those implementations used

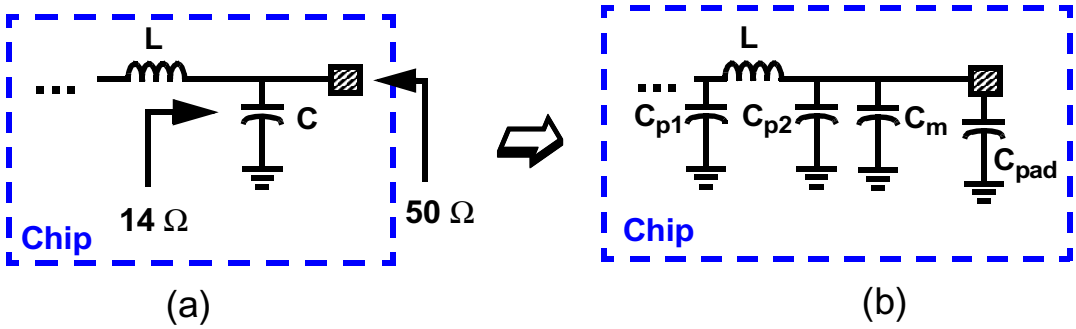


Figure 4-5 The on-chip impedance transformation network (ITN). (a) An ideal ITN, (b) ITN including parasitic capacitors.

off-chip components, and resulted degradation of the insertion loss. As the switch working frequency increases, the on-chip inductor Q can be sufficiently high to keep the loss associated with the inductor relatively low, and it should be possible to integrate the LC impedance transformation network (ITN). This reduces off-chip components and lowers cost.

An on-chip LC ITN is conceptually illustrated in Figure 4-5(a). The impedance looking into the chip is 50 Ω. The ITN reduces the impedance looking from the chip is to 14 Ω. Thus, the switch P_{1dB} can be improved by 5.5 dB. To realize this on-chip LC network, the parasitic capacitors from the inductor and pad as shown in Figure 4-5(b) must be considered. C_{p1} and C_{p2} are the parasitic capacitors of the inductor, C_{pad} is the capacitor from the pad and C_m is additional capacitor needed for the LC ITN. The on-chip LC ITN has two opposite effects on the switch insertion loss. First, the on-chip inductor and capacitor has finite Q and will introduce losses to the switch. The on-chip inductor also has parasitic capacitors (C_{p1} and C_{p2}). C_{p1} is not part of ITN and increases losses for the switch. As the on-chip impedance is reduced, the loss associated with the transistor increases. All these degrade the switch insertion loss. Second, the integrated LC ITN absorb the pad capacitance, i.e., the capacitance from the pad is part of the ITN. With the shielded pad, Q

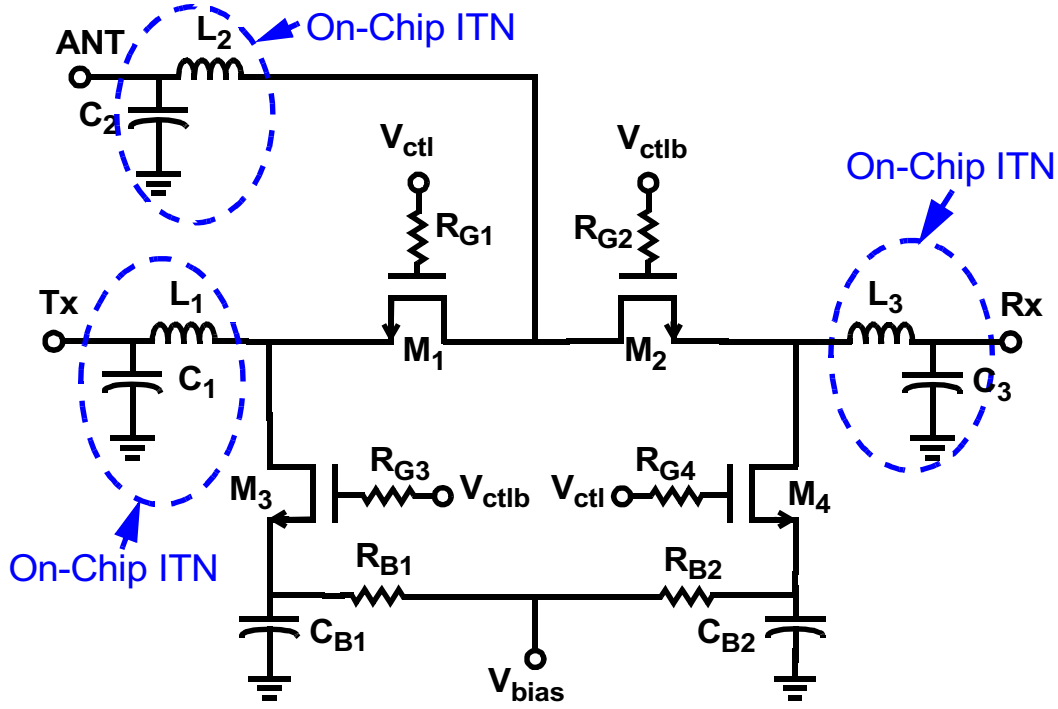


Figure 4-6 A schematic of 15-GHz CMOS switch with integrated impedance transformation networks.

of the pad could be high enough so that total Q of ITN is limited by the inductor. Thus the degradation of return loss through the pad can be eliminated. Since the return loss due to by pad capacitance is significant at high frequencies, the integrated ITN could improve the switch insertion loss. The design of on-chip LC ITN can balance these two opposite effects to keep the insertion loss almost the same, while, improving the switch P_{1dB}.

4.3.2 CMOS Switch with Integrated ITN

The schematic of 15-GHz CMOS switch with an integrated ITN's [34] is illustrated in Figure 4-6. Three ITN's are place in Tx, Rx and ANT nodes. The core of the switch employes the same topology as the switch without ITN described in section 4.2. The bias voltages are also the same thus these two CMOS switch can work with a single 3-V power supply, and do not need a voltage doubler which is required in the previously

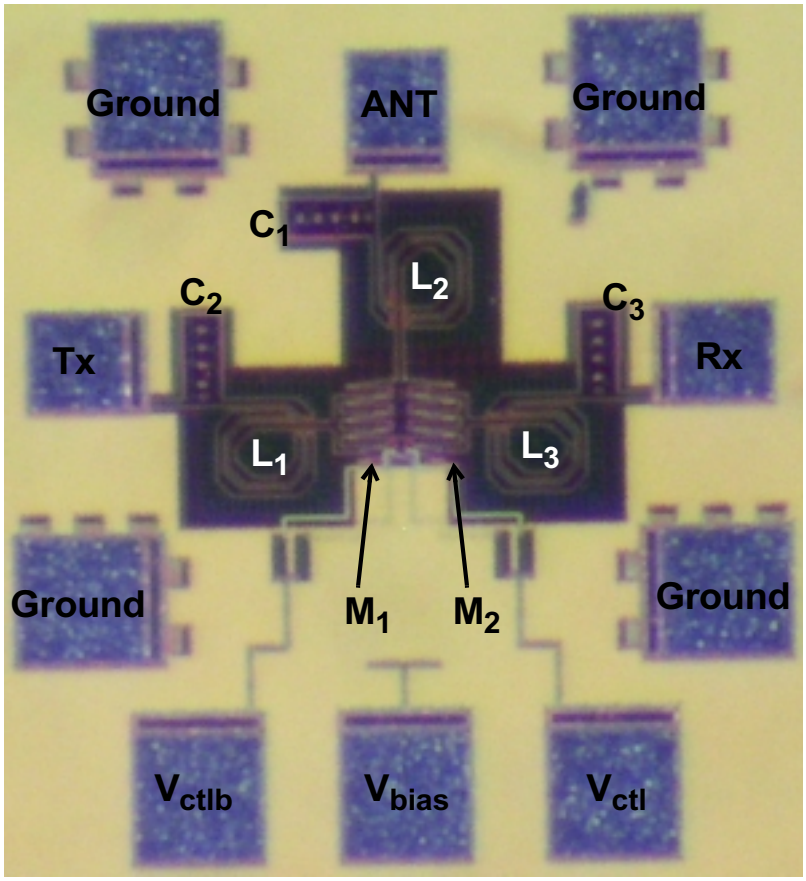


Figure 4-7 The die photo of the 15-GHz CMOS switch, with integrated LC impedance transformation networks.

reported CMOS switch as [21-23, 28]. Since the on-chip impedance is reduced, the transistor size is re-optimized to reduce the loss associated with transistors. Their sizes are 292/0.12 μm and larger than these of the switch without ITN's (91/0.12μm).

To increase the Q of ITN and minimize the loss associated with the inductor, the metal trace of inductors uses metal 3 to metal 8 layers shunted together. The simulated Q is higher than 30 at 15 GHz. On-chip capacitors are implemented using metal-to-metal parasitic capacitor structure. The simulated Q is higher than 200 at 15 GHz. To achieve the best insertion loss, the switch uses low substrate resistance layout [20-23]. The 80% of the die is covered by p^+ diffusion and substrate contacts. The die photo of this switch is shown

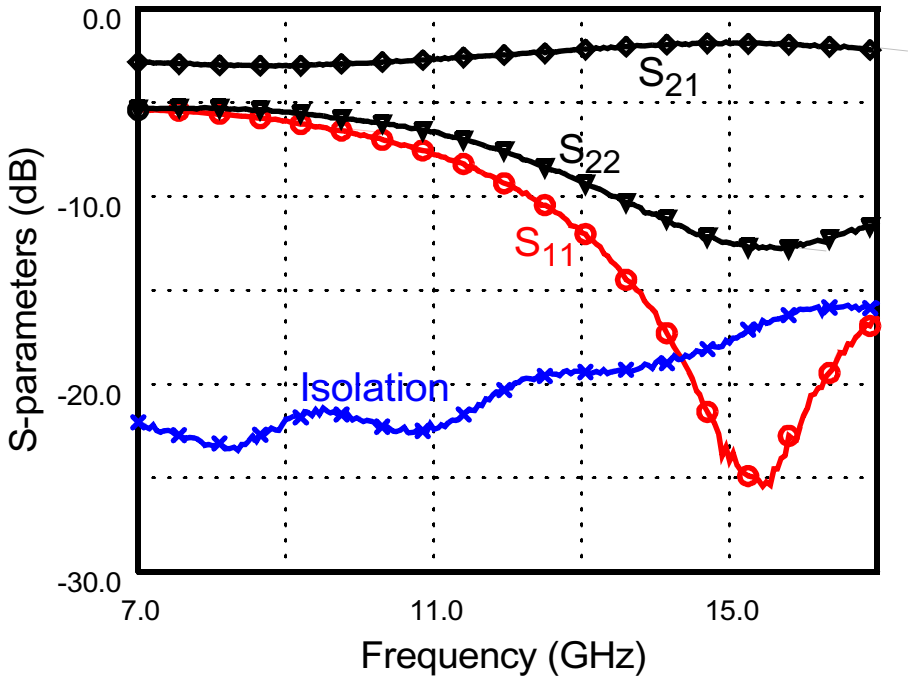


Figure 4-8 Measured S-parameters for the switch with integrated impedance transformation networks.

in Figure 4-7. The chip area is about 0.5 x 0.5 mm^2.

4.3.3 Experimental Results for CMOS Switches

The switch with ITN's has been characterized using an on-wafer setup. The measured switch S-parameters from 7 GHz to 17 GHz are plotted in Figure 4-8. The switch achieves the lowest insertion loss 1.8 dB at 15 GHz. When the switch is on, its return losses are tuned around 15 GHz. Both $|S_{11}|$ and $|S_{22}|$ have a pretty large -10-dB bandwidth of several giga Hertz. The measured $|S_{11}|$ and $|S_{22}|$ at 15 GHz are -24 and -12.5 dB, respectively. Here $|S_{11}|$ is measured at ANT node and $|S_{22}|$ is measured at either Tx or Rx node. Due to the large transistor size used in this switch, the switch isolation becomes low at high frequencies. The measured isolation is 17.8 dB at 15 GHz.

The power handling capability and linearity for the switch with ITN's are shown in Figure 4-9. The measured input IP3 is 34.5 dBm and input P_{1dB} is 21.5 dBm. Comparing

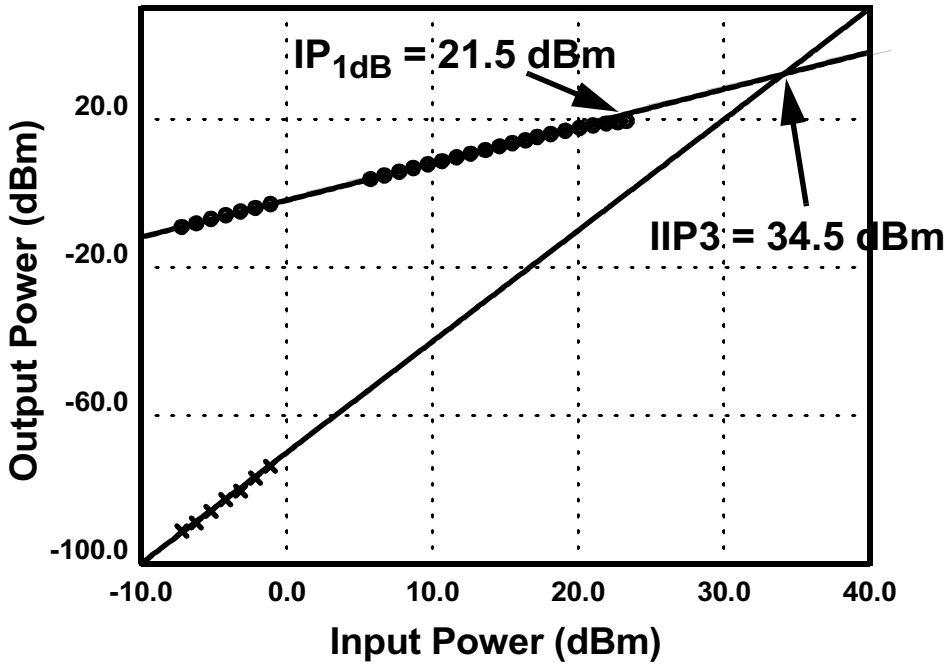


Figure 4-9 Measured P_{1dB} and IP3 for the switch with impedance transformation networks.

with the switch without ITN's, P_{1dB} improves 6.5 dB, but the insertion losses for the switches are the same. Thus, the advantage of integrated impedance transformation networks is obvious: it can improve the switch power handling capability (doubled the voltage swing at 50 Ω terminator) without any degradation of the switch insertion loss. Though, it has tuned frequency response, it can have excellent characteristic over several giga Hertz. Comparing to the switch without ITN's, its return losses are not good at low frequencies. But it can achieve good return losses at high frequencies where the switch without ITN's can not reach. The integrated ITN improves CMOS switch performance at high frequencies and provides more freedom in CMOS switch design.

The performance of two CMOS switches are summarized in Table 4-1. In order to provide more sense about the absolute performance of CMOS switch, the data for a GaAs switch, which is a MMIC switch from M/A com, are also included in the table. It shows

Table 4-1 Performances Summary of 15-GHz CMOS Switches and GaAs Switch

Switch	no ITN's	ITN's	GaAs
Insertion Loss (dB) at 15 GHz	1.8	1.8	1.6
Isolation (dB) at 15 GHz	23	17.8	42
Return Loss (dB) when the switch is on ($-S_{11}/-S_{22}$) at 15 GHz	8/9	24/12.5	20/20
Input P_{1dB} (dBm) at 15 GHz	15	21.5	25
Input IP3 (dBm) at 15 GHz		34.5	43
T_{on}, T_{off} (50%CTL to 90/10%RF)(nS)	0.5,0.25 (simulate)	1.2,0.8 (simulate)	3
Control Voltage (V)	3.0/1.2	3.0/1.2	0/-5
DC Current (mA)	0	0	50

that the CMOS switch with ITN's is competitive to the commercial GaAs switch. The switch with ITN's has 0.2 and 4 dB worse insertion loss and input P_{1dB} than GaAs switch, respectively. But, the GaAs switch requires negative 5V control voltage, which makes it difficult to use in commercial applications. The CMOS switches only require a single 3-V power supply. The simulated switching time for the switch with ITN's is 1.2 nS. Comparing to the 3 nS measured switching time of GaAs switch, it has margin. Both switches achieved good return loss at 15 GHz.

The only specification which the GaAs switch has significantly better performance than the CMOS switches is isolation. The measured isolation of GaAs switch is 26-dB better than the switch with ITN. Due to the lossy nature of silicon substrate, CMOS switches usually do not have good isolation at high frequencies. But what really determines the CMOS switch isolation? More analyses are given in the next section.

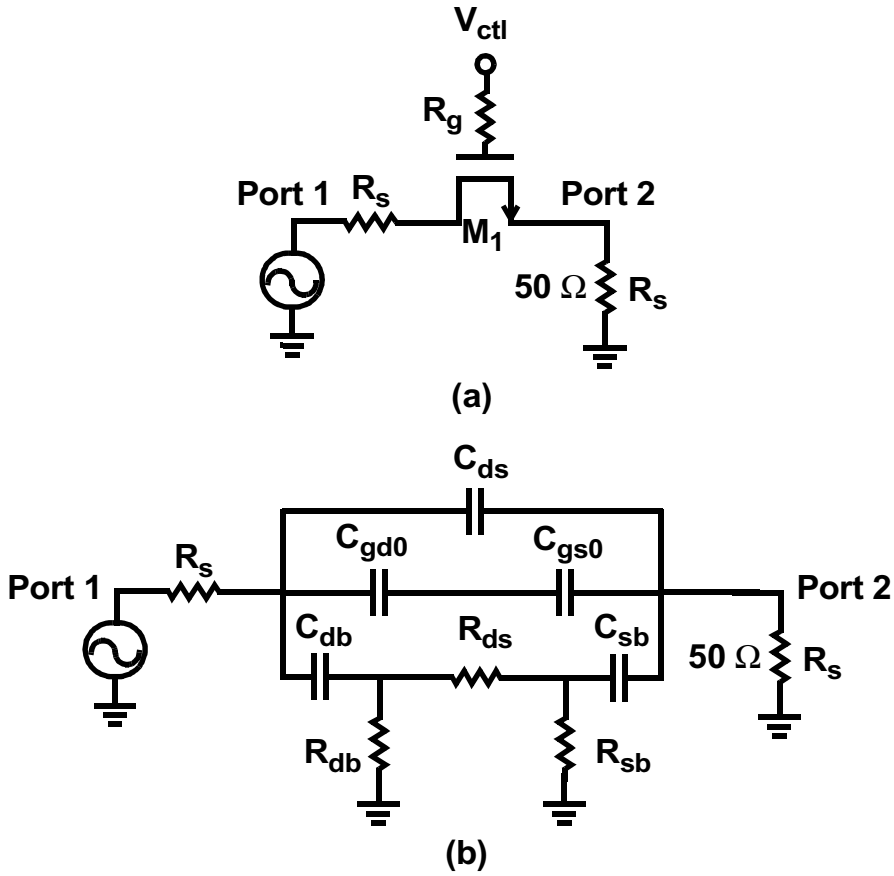


Figure 4-10 Single MOS transistor switch, (a) the schematic, and (b) its equivalent isolation model

4.4 CMOS Switch Isolation

Instead of analyzing a complicated four-transistor switch, a single NMOS transistor switch shown in Figure 4-10(a) is used here to demonstrate the switch isolation problem without losing generality. R_g is the gate resistor and R_s is the 50-Ω characteristic impedance. When the transistor is off, the conductive channel under the gate disappears, thus at low frequencies the two ports should be perfectly isolated. But associated with the switch structure, there are parasitic capacitances, resistances and inductances. In order to clearly illustrate these parasitics, a cross-section of the switch transistor is shown in Figure 4-11.

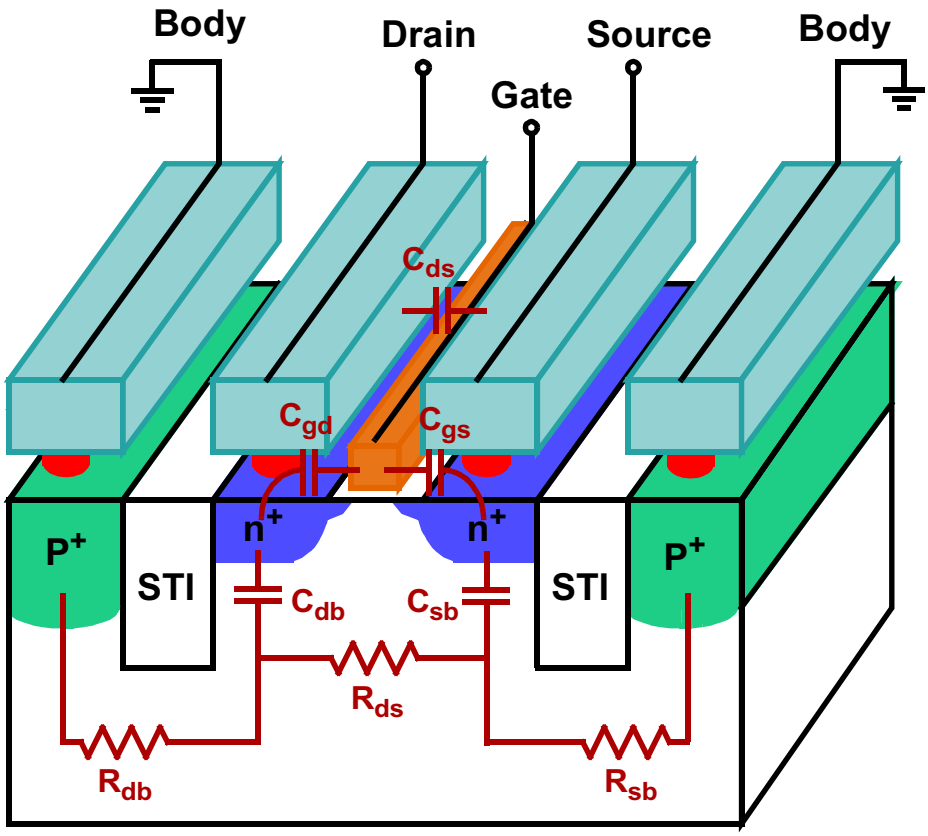


Figure 4-11 NMOS transistor cross section with parasitics

A capacitor directly coupling the transistor drain and source is C_{ds}, which is resulted from the fingered interconnection structure [35]. As CMOS dimensions continue shrinking and more metal layers are stacked for interconnection, this capacitance becomes a much more critical factor for switch isolation. Because the transistor gate to body capacitance usually is small and the resistor between the gate and control voltage is large (~5 kΩ), the transistor gate node can be considered as open. Thus, the parasitic gate to drain capacitor (C_{gd}) and gate to source capacitor (C_{gs}) are in series between the drain and source. Since the transistor is off, these two capacitors are mostly from the overlap and fringe capacitance. So C_{gd} and C_{gs} can also be expressed as C_{gd0} and C_{gs0}, respectively. The transistor drain and source have the parasitic junction capacitances to body, C_{db} and

C_{sb}. These two parasitic capacitors are connected to the grounded body through the spreading substrate resistors. The R_{ds} represents the substrate resistance underneath the drain and source. R_{db} represents the substrate resistance between the p^+ body diffusion and C_{db}. R_{sb} is the substrate resistor between the body and C_{sb}. With all these parasitic capacitors and resistors included, a complete switch isolation model then is shown in Figure 4-10(b).

In order to increase switch isolation, all parasitic capacitances have to be reduced. The C_{db} and C_{sb} are n^+-to-p-sub junction capacitors and can be reduced by reversely biasing the drain and source. C_{gd0} and C_{gs0} are proportional to the transistor size, which is mainly determined by the switch insertion loss. C_{ds} is also proportional to the transistor size. But it can be reduced by using fewer metal layers stacked on the top of the drain or source. The trade-off is that when the lower metal is used to connect the drain or source out, the parasitic capacitance between the drain/source to the body increases. This in turn impairs the switch insertion loss.

The substrate resistance also affect the switch isolation. With fixed parasitic capacitance, the switch will achieve the worst isolation if R_{ds} is zero while R_{db} and R_{sb} are infinite. R_{ds} is not a free design variable. It is proportional the transistor size. With contemporary CMOS technology, R_{ds} usually is small for the transistor size needed for the best insertion loss. For example, in 0.13-μm CMOS technology, the measured R_{ds} at DC is about 19 Ω for a 91/0.12 μm transistor. Thus, in order to achieve better isolation, R_{db} and R_{sb} have to be lowered. This observation agrees with the measured isolation characteristics of 5.8-GHz CMOS switch [23] discussed in Chapter 3. The switch with very high substrate resistance has ~2-dB worse isolation than the switch with lower substrate resistance.

From the switch isolation model in Figure 4-10(b), it is obvious that when the switch is off, the main signal path between port 1 and port 2 is through the parasitic capacitors. In the 15-GHz CMOS switch designs, the simulation indicates that the presence of C_{ds} degrades the switch isolation about 12 dB at 15 GHz. Techniques to improve CMOS switch isolation at high frequency should continue to be investigate.

4.5 Conclusion

Two 15-GHz CMOS switches have been fully integrated in a 0.13-μm CMOS foundry process. One is designed with on-chip LC impedance transformation networks (ITN's) and the second one without ITN's. The switches achieves the same 1.8-dB insertion loss at 15 GHz, but 15 and 21.5-dBm input P_{1dB} for the switches without and with ITN's, respectively. The degradation of insertion loss due to the use of ITN's is offset by reducing the return loss through the bond pad capacitances in the switch without ITN's. The switch with ITN's is the first CMOS switch operating at 15 GHz with competitive performance as commercially available GaAs switches. The switch without ITN's is the first CMOS switch suitable for the Ultra-Wide Band (UWB) applications. Both switches work with 3V/1.2V control voltages without using a voltage doubler. Integrated ITN's provide a mean to improve CMOS switch power handling capability at high frequencies. However, CMOS switch with ITN's exhibits 26-dB lower isolation than the GaAs switch. To understand the CMOS switch isolation model, parasitics associated with the CMOS switch also have been analyzed.

CHAPTER 5
A WIDE TUNING RANGE VCO AND CMOS DIVIDERS

5.1 Introduction

As discussed in Chapter 2, the second voltage controlled oscillator in the multi-band receiver (Figure 2-7) needs over 45% tuning range in order to take the advantage of the first fixed frequency LO (VCO1). In contemporary bulk CMOS technology, LC VCO tuning ranges are around 10 to 30% [36]-[39]. Without any special techniques, a VCO tuning range is usually limited by the varactor which is difficult to have a large tunability with acceptable quality factor (Q) in bulk CMOS technologies. Defining varactor tunability as C_{max}/C_{min} [40], tunability of 2.45 with minimum Q of 20 at 1GHz is reported [40] in a 0.5-μm CMOS process. Wong [41] reports a three-terminal varactor with a tunability of 3.3 and minimum Q larger than 10 at 2GHz in a 0.35-μm CMOS process. A larger tunability of 5.3 could be achieved with process modifications [42], but this structure is not available in a standard foundry CMOS process.

The required wide tuning range VCO can be achieved by using a ring oscillator, but it usually has poor phase noise [43]. On the other hand, use of an LC-VCO with a wide tuning range requires high VCO gain (MHz/V), especially at low supply voltages, which subsequently renders VCO more susceptible to the voltage noise induced phase noise increases [39]. Furthermore, achieving good phase noise over the entire frequency range is difficult.

In this VCO design, switched resonators [44,45] are utilized to augment the tuning range. A 53% tuning range VCO [45] has been developed which covers between 700 and 1100 MHz as required in the system design. At 1.5 V power supply voltage, the VCO achieves -123 dBc/Hz phase noise at a 600 kHz offset frequency over the whole tuning range. The VCO was fabricated in a 0.18-μm foundry CMOS process, the design of the VCO is presented in section 5.2. A CMOS divider working with the VCO to generate 350 – 550 MHz quadrature signals required by the system (LO2) is described in section 5.3.

5.2 A 900-MHz Wide Tuning Range CMOS VCO

5.2.1 VCO Small Signal Model

The VCO employes a cross-coupled PMOS differential pair with LC tanks. The simplified VCO core schematic is shown in Figure 5-1(a), It includes on-chip inductors and on-chip varactors. The load (Z_{load}) usually is the input of CMOS buffer circuits which is capacitive. The equivalent circuit model of the VCO is shown in Figure 5-1(b), where the broken lines in the middle represent either a common mode node or ground. The symmetric planar spiral inductor model of Figure 5-1(c) with identical RC loading on both terminals is used as a part of the tank model. The parasitic capacitance of inductors is represented by C_L, which is equal to $2C_s+C_p$. R_s is the parasitic resistance in series with inductance L. R_p represents the shunt resistance across the port and ground. The quality factor (Q_L) of the L-R series combination is then given by $Q_L=(\omega L)/R_s$, where ω is the operation frequency.

Varactors are modeled with a capacitor C_v in series with a resistor R_v. In a similar way, output load is defined using a series combination of C_{load} and R_{load}. The quality fac-

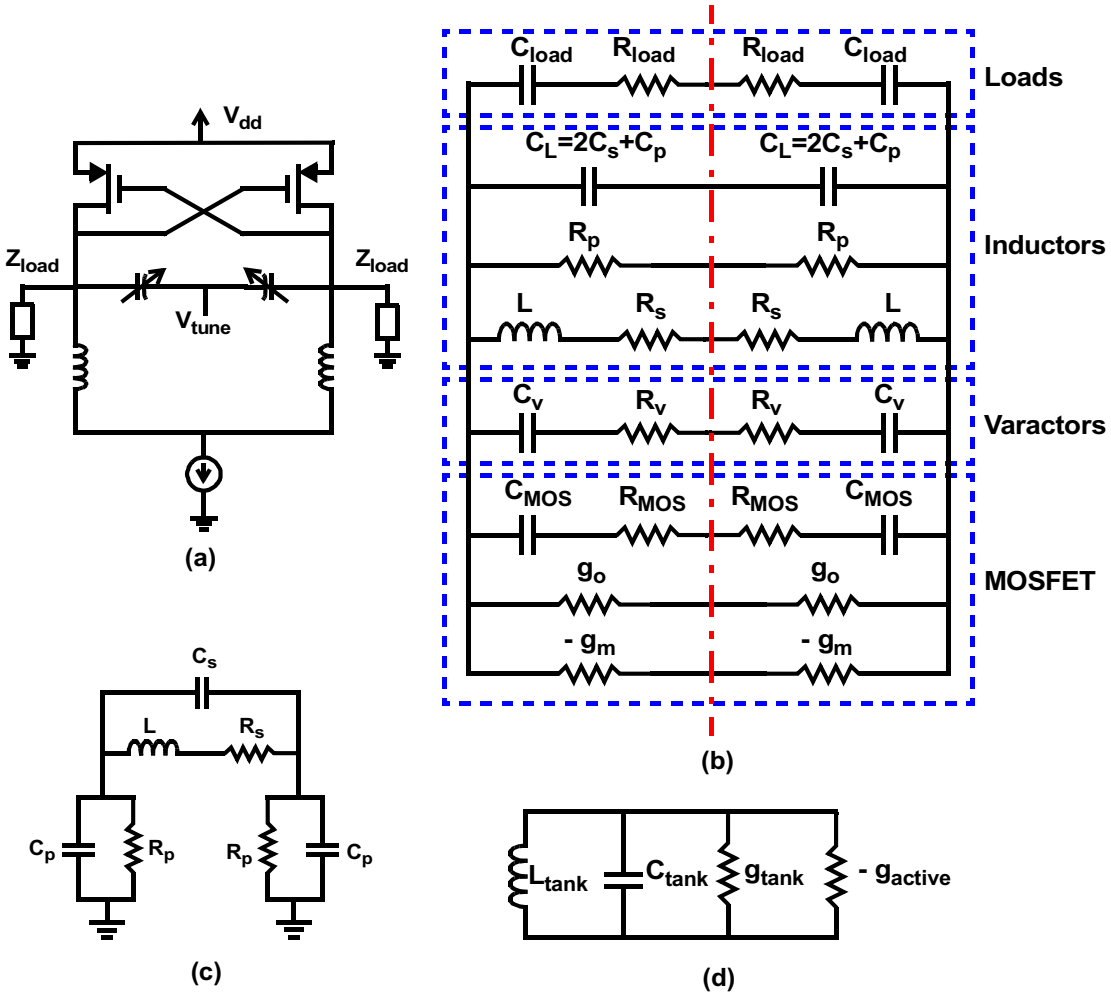


Figure 5-1 VCO small signal model. (a) Simplified VCO circuit schematic, (b) the equivalent small signal model for VCO, (c) equivalent circuit model for inductors and (d) a parallel LC oscillator model

tor for a capacitor (Q_C) is given as $Q_C = 1/(\omega RC)$, where ω is the operation frequency, R is the parasitic resistance in series with capacitance C.

The parasitic capacitances from a MOS transistor is described as C_{MOS}, which includes C_{db}, C_{gs}, C_{gb} and C_{gd}. The series resistance R_{MOS} is mainly due to the substrate resistances associated with source/drain to substrate junction (C_{db}/C_{sb}) and gate to substrate (C_{gb}) capacitors [46]. Large area substrate contacts are necessary to lower R_{MOS} to

improve the quality factor of C_{MOS}. g_m and g_0 are small-signal transconductance and output conductance of the transistors, respectively.

A VCO small signal equivalent circuit model including models of inductors, varactors, MOSFETs and loads is shown in Figure 5-1(b). This model can even be simplified as a parallel LC oscillator model as illustrated in Figure 5-1(d). Four parameters are used to described a VCO circuit [47]: the loaded tank loss g_{tank}, effective negative conductance $-g_{active}$, tank inductance L_{tank} and tank capacitance C_{tank}. g_{active} is solely provided by the transistor transconductance, where:

$$2g_{active} = g_m . \tag{5.1}$$

If Q's of inductors and any capacitors (parasitic capacitors or varactors) are large enough (> 4), the L_{tank} and C_{tank} are approximately given as

$$L_{\tan k} = 2L \tag{5.2}$$

$$2C_{\tan k} = C_{MOS} + C_L + C_v + C_{load} . \tag{5.3}$$

The loaded tank loss g_{tank} is due to the loss of transistor output conductance (g_0), transistor parasitic capacitance loss (g_{MOS}), inductor loss (g_L), varactor loss (g_v) and output load loss (g_{load}). Thus,

$$2g_{load} = g_o + g_{MOS} + g_L + g_v + g_{load} . \tag{5.4}$$

The g_{MOS}, g_v, and g_{load} can be calculated from the general *RC* loss equation as $g = C\omega / Q_C$, here C is capacitance from MOS, varactor or output load, and Q_C is their respective quality factor.

The loss from inductors g_L is usually the dominant term and is

$$g_L = 1/R_p + R_s/(L\omega)^2 \approx R_s/(L\omega)^2 , \tag{5.5}$$

if $1/R_p$ is much smaller than the other term, which usually is the case.

The VCO operation frequency ω is determined by L_{tank} and C_{tank}. At desired ω, the integrated VCO has to be optimized with minimum losses of g_0, g_{MOS}, g_L, g_v and g_{load}. In bulk CMOS technology, at frequencies lower than ~5 GHz, the dominant lossy term is g_L, i.e., inductor loss.

One criterion for oscillation is $g_{active} = g_{tank}$. The transistor transconductance to satisfy this criterion is $g_{m,min}$. In order to guarantee oscillation, also to have sufficient tank voltage swing to lower phase noise, each transistor must have transconductance $g_m = k \cdot g_{m,min}$, where k is ~ 2 – 4 [36]. If only inductor loss is included in g_{tank}, then

$$g_m = k \cdot \frac{R_s}{(\omega L)^2} = k \cdot \frac{1}{Q_L^2 \cdot R_s} = k \cdot \frac{1}{Q_L \omega L}. \qquad (5.6)$$

A VCO tuning range solely determined by MOS varactors can not be large unless SOI CMOS technology is used [48]. One way to increase an LC-tuned VCO tuning range is to use switched capacitors [37,49]. In this technique, additional switched capacitors augments VCO tuning range while VCO inductance is kept the same. But from Eq. (5.6), if ω change is large, e.g. 550/350 = 1.6 in the multi-band receiver, g_m must vary as ω^{-2}, e.g. ~1/2.6 here, with fixed L and R_s. In saturation region of operation, MOS g_m varies as approximately square root of drain current. Thus drain current has to change by ~ 6.6 over the tuning range. Since typically, bias condition is not continuously varied, so, most of the current is wasted at the high frequency end if the VCO bias is optimized for the low frequency operation. Since low power consumption is important in wireless LAN applications, the use of only switched capacitors is probably not the best approach for implementing a wide tuning range VCO.

In Eq. (5.6), if ω and L can be simultaneously changed, g_m thus power consumption can be optimized for the two ends of tuning range. The switched resonator, in which both inductance and capacitance can be simultaneously changed, and its use to realize a wide tuning range VCO is described in the next subsection.

5.2.2 Switched Resonator Concept

A high tuning range VCO with inductance tuning has been proposed [50]. However, the VCO has with very poor phase noise performance. As mentioned, in this work, the switched resonator concept [44] illustrated in Figure 5-2 is utilized to increase the tuning range and to achieve low phase noise over the tuning range at reasonable power consumption. The inductance seen between ports 1 and 2 are changed by turning M_1 on and off. When the transistor is off, the inductance is approximately the sum of L_1 and L_2. The

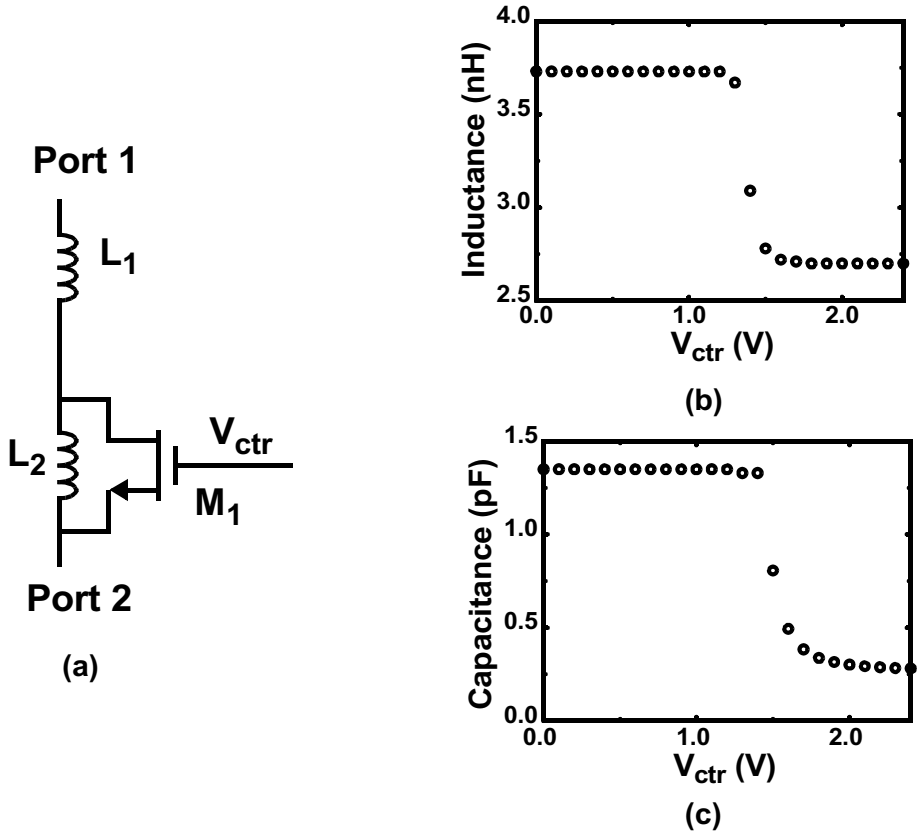


Figure 5-2 The switched resonator. (a) A schematic, and simulated (b) inductance, (c) capacitance

actual combined inductance is somewhat lower due to the effects of C_{gd} in series with C_{gs}, and C_{db} of M_1 [44]. These capacitances also affect the capacitance seen from port 1 (C_{p1}). When M_1 is on, L_2 is shunted out and the inductance is decreased as also shown in Figure 5-2. Furthermore, when M_1 is on, C_{p1} is reduced because the transistor capacitances and the capacitances associated with L_1(partially) and L_2 are shunted to ground by the low on resistance of M_1, thus, leading to simultaneous decreases of inductance and capacitance. This ability to simultaneously tune both *L* and *C* provides greater flexibility to trade-off phase noise and power consumption, as well as to achieve given phase noise performance over a larger frequency range [44] compared to using only switched capacitors [37,49].

5.2.3 Circuit Design of Wide Tuning Range VCO

The VCO schematic is shown in Figure 5-3, which is similar to Yim [44] and

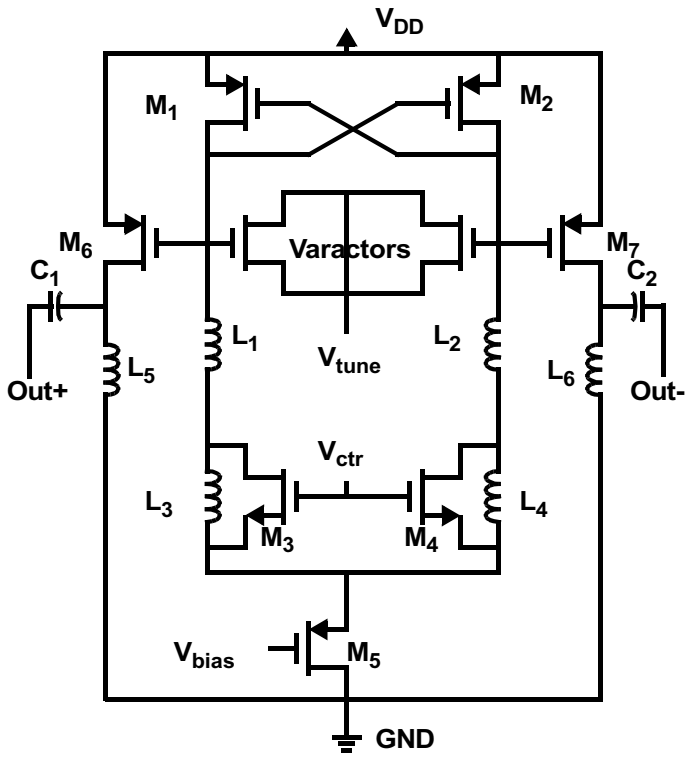


Figure 5-3 A schematic of 900-MHz voltage-controlled oscillator

Hung [38]. M_1 and M_2 form a cross-coupled PMOS pair and provide negative resistances ($-2/g_m$) in the VCO core. The PMOS, M_5 is used to set the current for the VCO.The transistor sizes are 300/0.18 μm for M_1, M_2 and 2000/0.18 μm for M_5. Having this large size for M_5 reduces 1/f noise in the tail transistor and thus the close in phase noise of the VCO. These sizes set the voltage at the source of M_5 ($V_{s,M5}$) to almost 1/2 V_{dd} when M_5 drain current is 14 mA. M_6 and M_7 form output buffers. The buffer inductors, L_5 and L_6 are low Q to provide flat response over the operating frequency range for the VCO. Output capacitors C_1 and C_2 are 4 pF MOS capacitors, which provide matching to 50 Ω in conjunction with L_5 and L_6. The LC tanks include MOS varactors, inductors and switched resonator transistors M_3 and M_4.

The inductors, L_1 and L_2 are 2.5nH inductors and L_3 and L_4 are 1.2 nH inductors. The inductors have patterned ground shields [51,52] and are formed by shunting metal 4,5, and 6 layers. The metal lines are 15 μm wide and the space between metal lines is 3 μm. When control voltage (V_{ctr}) is low, i.e., the switching transistors M_3 and M_4 are off, the total inductance of the tanks is around 2.5+1.2=3.7 nH. When V_{ctr} is high, M_3 and M_4 shorts out L_3, and L_4, then the total inductance is 2.5 nH. Figure 5-2 shows the how the inductance and capacitance are changed with the control voltage. When M_3 and M_4 are on, the on-resistances of M_3 and M_4 are in series with L_1 and L_2, respectively, which increases total series resistances of L_1 and L_2 and thus lowering inductor Q. In order to keep this detrimental effect as small as possible, a large NMOS transistor is used for M_3 and M_4, and V_{ctr} is set to switch between 0 and 2.4 V. The V_{ctr} = 2.4 V is safe here because $V_{s,M5}$ is 0.75 V and V_{gs} =2.4-0.75=1.65 V, which is less than the 1.8-V supply

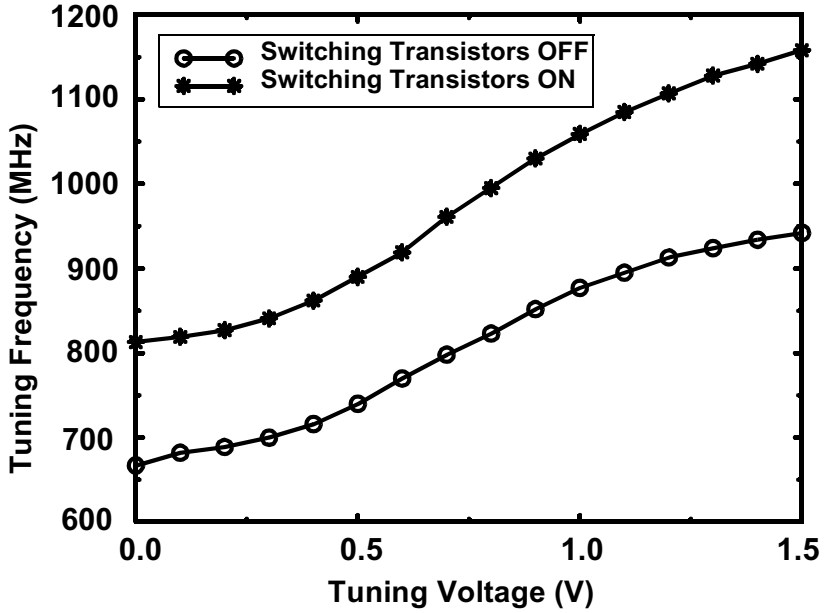


Figure 5-4 Measured VCO tuning characteristics: coarsely tuned by switching inductors and finely tuned by varactors

voltage for the 0.18-μm CMOS process. When the size of M_3 and M_4 are 2000/0.18 μm, simulations show that the on-resistance is 0.4 Ω.

The varactors are implemented using the accumulation mode MOS structure [53] and laid out using a differential architecture [40]. The capacitance is about 10 pF for each varactor.

5.2.4 Experimental Results

The VCO measurements were performed on-wafer. It operates between 667 MHz to 1156 MHz. It has a 53.6% tuning range. As illustrated in Figure 5-4, the VCO is coarsely tuned with the switched resonators and finely tuned using the MOS varactors. When the switching transistors M_3 and M_4 are off, i.e., when V_{ctr} is low, by changing the MOS varactor tuning voltage (V_{tune}), the output frequency is varied from 667 MHz to 942 MHz (band 1). When the switching transistors are on, the varactor tunes VCO from 813 MHz to 1156 MHz (band 2). The average VCO gains are 183 MHz/V and 228 MHz/V for

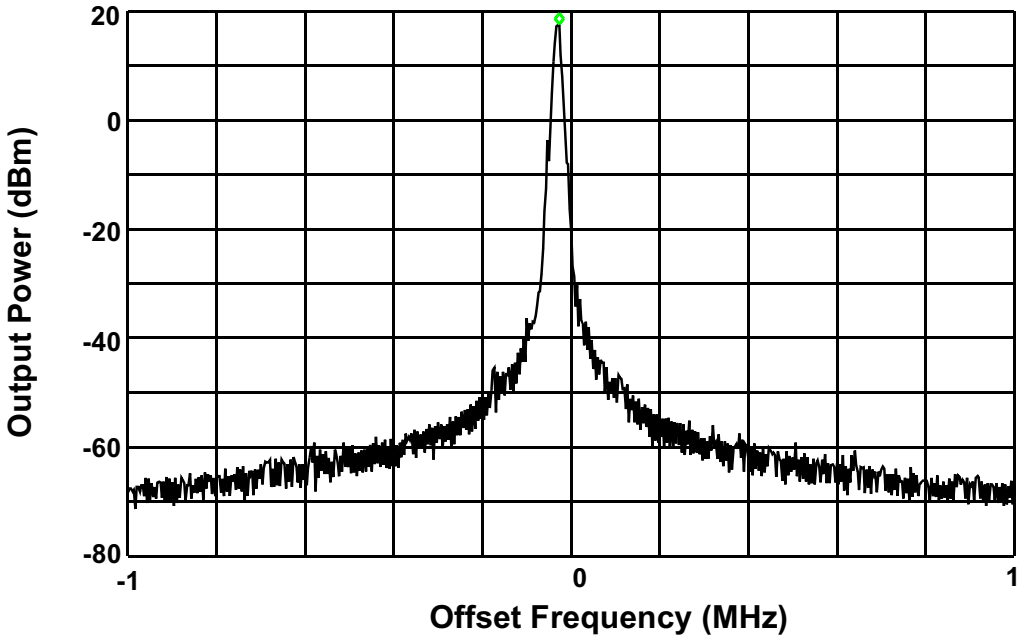
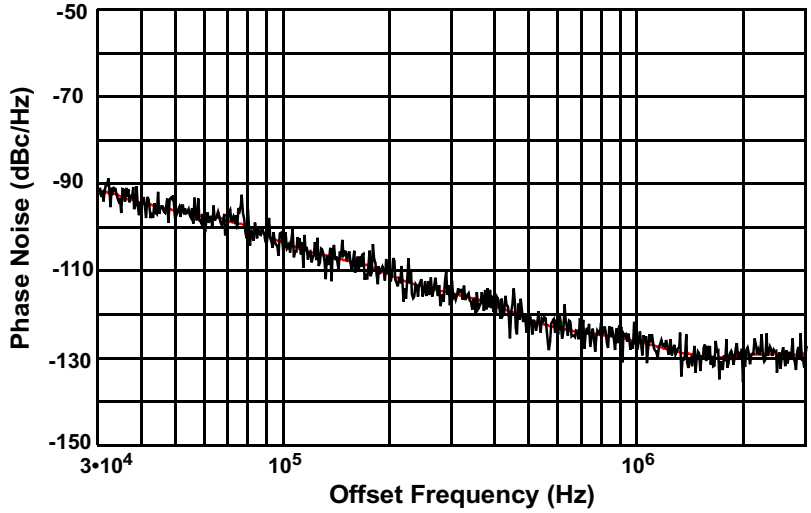


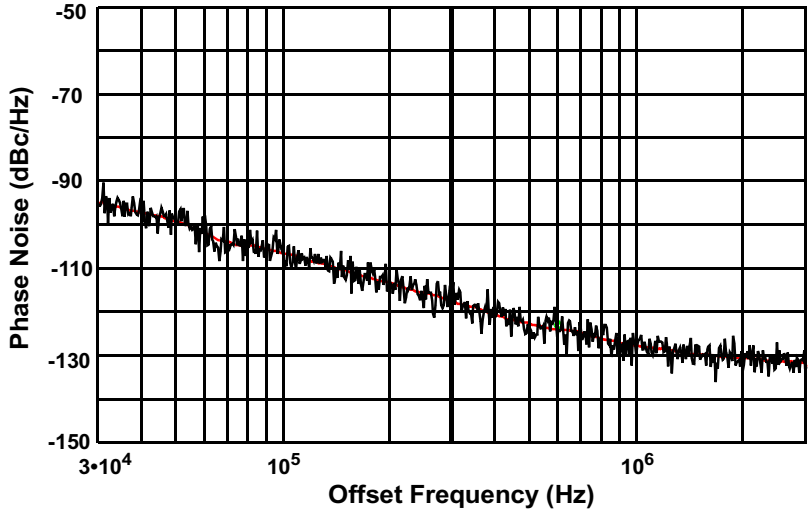
Figure 5-5 Measured VCO output spectrum at 1125 MHz

band 1 and 2, respectively. There is a 130-MHz overlap between band 1 and band 2. This overlap ensures the continuity of tuning despite the process and temperature variations. If the overlap is reduced, e.g. from 130 MHz to 50 MHz, even a larger tuning range can be realized.

The VCO phase noise was measured using a spectrum analyzer. At the supply voltage of 1.5 V, VCO output power is about -1.67 dBm at the 1127 MHz center frequency. The VCO core draws about 14 mA current, while the VCO buffers draw about 3 mA from a 1.5 V power supply. To improve measurement sensitivity, a power amplifier is added between the VCO output and spectrum analyzer. A VCO output spectrum is shown in Figure 5-5 when the center frequency is 1125 MHz with a span of 2 MHz. VCO phase noise plots are given in Figure 5-6: (a) when the center frequency is 1125 MHz, which is obtained by setting V_{ctr}=2.4 V and V_{tune}=1.5 V, and (b) when the center frequency is 666 MHz at V_{ctr}=V_{tune}=0 V. The phase noises at a 600 KHz offset for (a) and (b) are -123.1



(a)



(b)

Figure 5-6 Measured VCO phase noise using spectrum analyzer at (a) 1125 MHz and (b) 666 MHz.

dBc/Hz and -124.2 dBc/Hz, respectively, which are good. Figure 5-7 shows the phase noise at a 600 kHz offset versus oscillation frequency. The phase noise is essentially flat over the entire operating frequency range.

Table 5-1 summarizes phase noise performances for bands 1 and 2. As mentioned earlier, when switching transistors M_3 and M_4 are on, additional series resistances arising from the transistors could increase VCO phase noise. The conditions (b) and (c) attempted

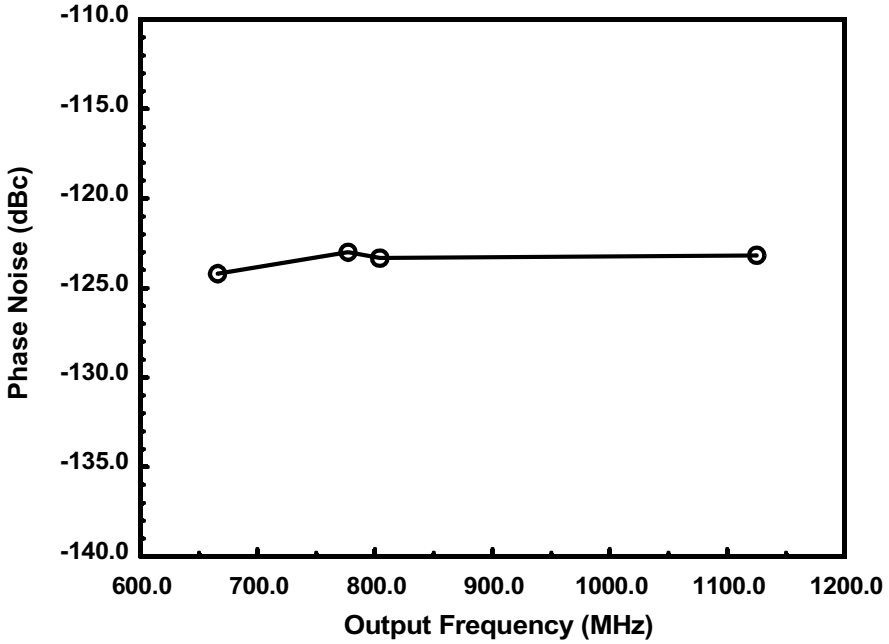


Figure 5-7 Measured VCO phase noise versus output frequency

Table 5-1 Summary of measured VCO characteristics

	(a)	(b)	(c)	(d)
V_{ctr} (V)	2.4	2.4	0	0
V_{tune} (V)	1.5	0	0.8	0
Centre frequency (MHz)	1125	804	777	666
Phase Noise at 600 KHz offset (dBc/Hz)	-123.1	-123.3	-123	-124.2
Core Current (mA)	14.1	14.5	14.5	14.4

to tune the VCO at the same frequency with the switching transistors on (case (b)) and off (case (c)). Surprisingly, the resulting phase noise difference is less than 0.3 dB which is well within the typical measurement tolerances. It appears that the on-resistances and other losses associated with the switch transistors have been made sufficiently low.

Figure 5-8 is a VCO chip micro-photograph. It occupies 1100x860 μm^2 area.

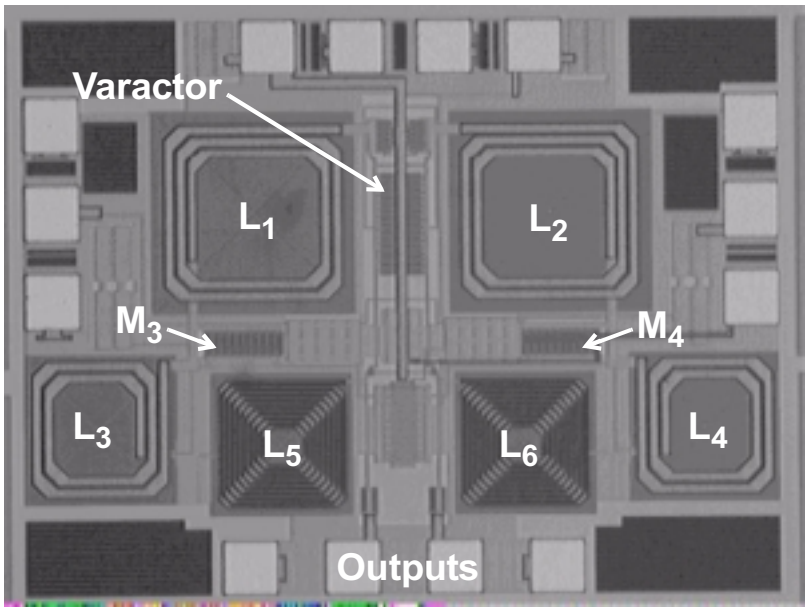


Figure 5-8 VCO chip micro-photograph

5.2.5 Summary

A 900-MHz monolithic VCO implemented in a 0.18-μm foundry CMOS process is presented. When operated with an 1.5 V power supply, it achieves a 53.6% tuning range. Switched resonators were employed for coarse tuning while MOS varactors are used for fine tuning. Nearly constant phase noise was observed over the entire tuning range between 667 MHz to 1156 MHz. The phase noise at a 600 kHz offset is -123.1 dBc/Hz at the 1125 MHz center frequency, -124.2 dBc/Hz at the 666 MHz center frequency and approximately -123 dBc/Hz at the 800 MHz center frequency. At an 100 kHz offset, phase noise is around -109 dBc/Hz which is excellent. If -30 dB/decade slope is assumed for lower offset frequency, phase noise is -79 dBc/Hz at a 10-kHz offset.

This VCO has a sufficient tuning range and margins to be used for the 802.11 wireless LAN applications and it covers the frequency range required by multi-band receiver discussed in Chapter 2. The phase noise measurements at 100 and 600 kHz off-sets indicate that the VCO should be adequate for this application.

5.3 VCO with Divider as Quadrature Generator

As discussed in Chapter 2, a divider is used to generate quadrature signals for LO2. A source coupled logic (SCL) divider which is also called current-mode logic (CML) divider is employed here.

A divider schematic is illustrated in Figure 5-9. The divider takes the outputs of VCO described in the last section as its inputs, and generates four outputs: a pair of differential quadrature signals (q and qb) and a pair of differential in-phase signals (i and ib). This type of divider has been intensively studied in the SiMICS group of UF and design details can be founded in Hung [46], Floyd [54] and Li [55]. The VCO described in last section and this divider were integrated into a single die. A PMOS source follower circuit is inserted between the VCO core and divider to provide isolation between the two circuits and to buffer the VCO outputs. To drive off-chip measurement equipments, inverters are utilized as buffers at the divider outputs.

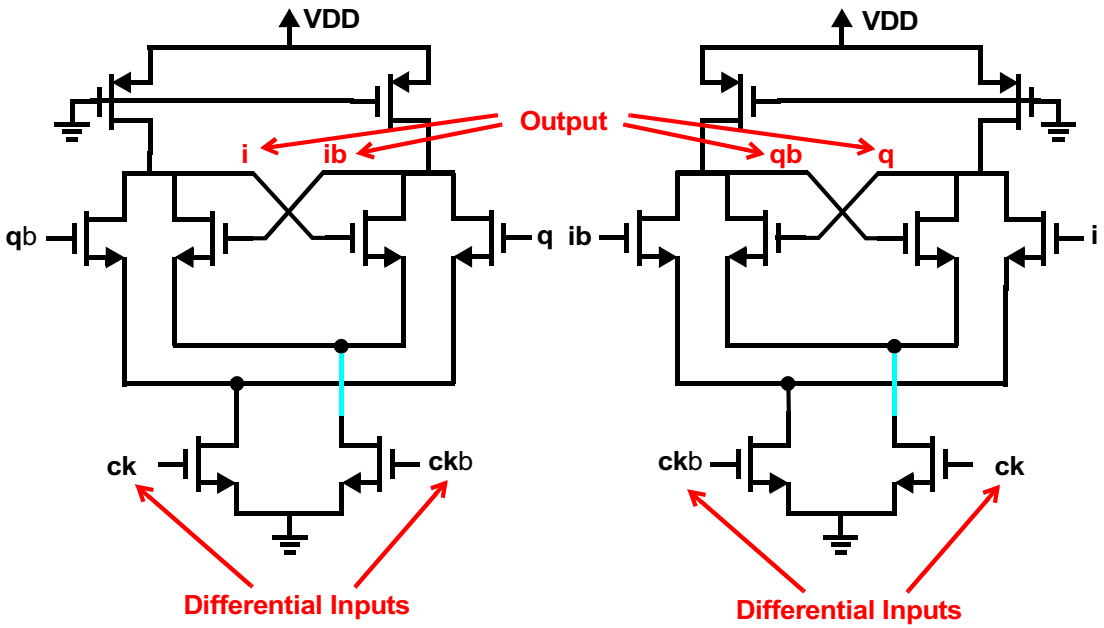


Figure 5-9 A schematic of divided-by-2 circuits, it takes a differential inputs from the VCO and generates differential I and Q outputs

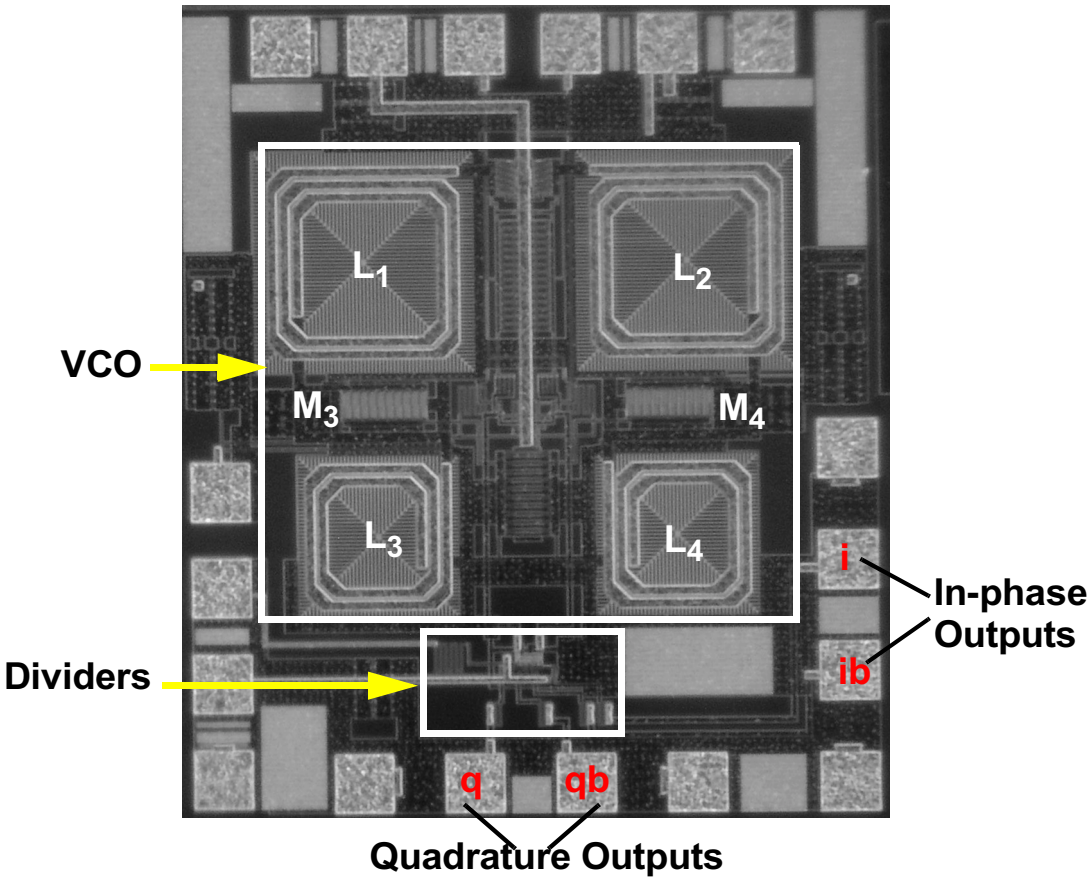
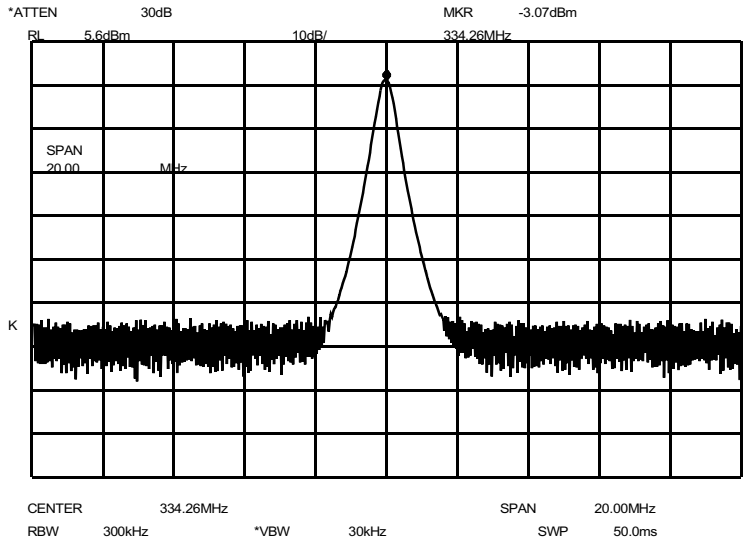


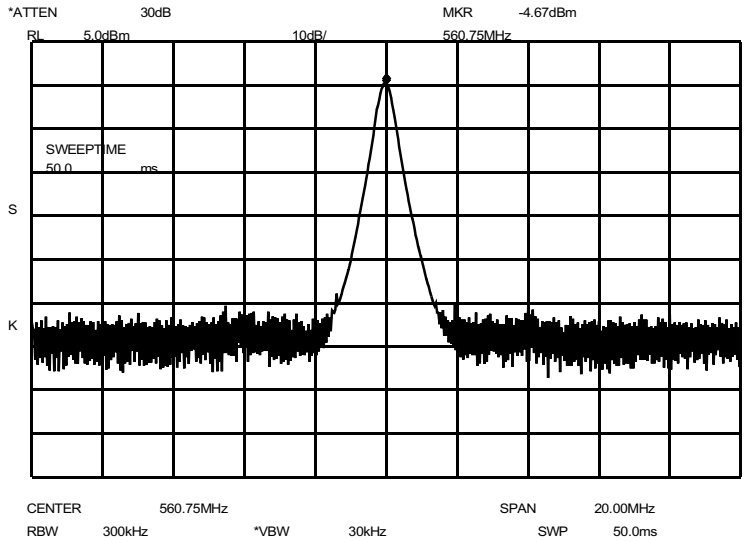
Figure 5-10 A die photograph of VCO and divider, both sine and cosine waves are generated at divider outputs.

A die photograph of VCO and divider is shown in Figure 5-10. The VCO core is the same as that shown in Figure 5-3. The divider outputs are both sine (quadrature) and cosine (in-phase) signals as marked in the die photo.

The VCO and divider circuits are tested on-wafer. The divider clearly functions as a divided-by-two circuits. The output spectrum are shown in Figures 5-11 (a) and (b) which illustrates the divider output when the VCO runs at its lowest frequency, e.g. the switching transistor is off and V_{tune} = 0 V, and which shows the divider output when the switching transistor is on and V_{tune} = 1.5V. The output frequencies as a function of the VCO control voltages are summarized in Table 5-2. Table 5-2 clearly demonstrates that the divider outputs is at the half frequencies of the VCO outputs.



(a)



(b)

Figure 5-11 Divider outputs when VCO runs at its (a) lowest frequency and (b) highest frequency.

Table 5-2 Measured divider output frequencies as VCO control voltages

V_{ctr}	V_{tune} (V)	Measured VCO frequency in Figure 5-5 (MHz)	Measured divider output frequency (MHz)
Low	0	667	334
Low	1.8	942	466
High	0	813	397
High	1.8	1156	561

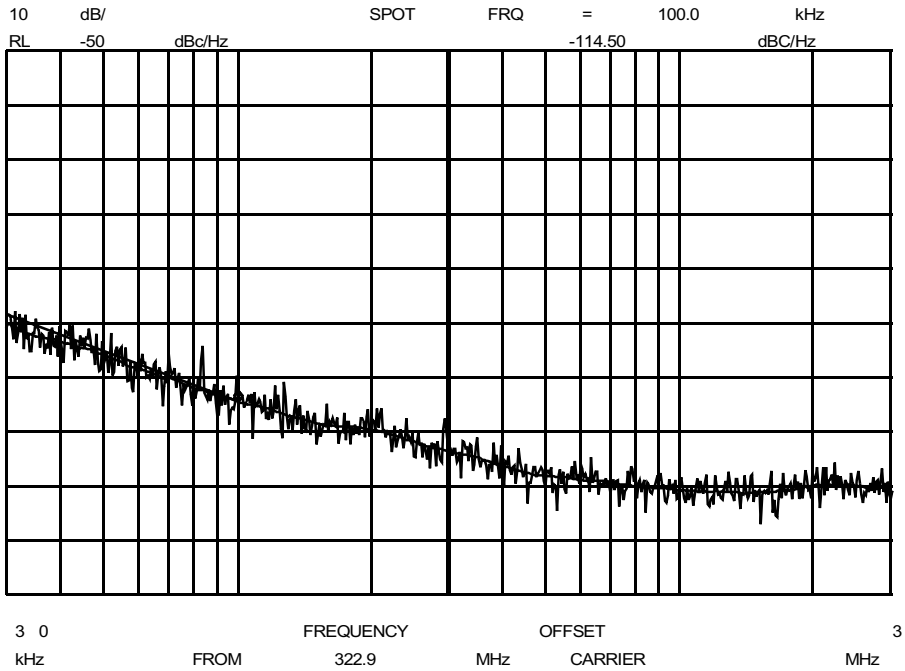


Figure 5-12 Measured VCO and divider phase noise at 323 MHz. The phase noise is -114.5 dBc/Hz at 100 kHz offset.

The phase noise of the VCO-divider combination is also measured. Figure 5-12 illustrates the phase noise when the divider output is 332 MHz. At 100 kHz offset, the measured phase noise is -114.5dBc/Hz, and at 30 kHz offset, phase noise is ~ 100 dBc/Hz. The -86 dBc/Hz phase noise at 10 kHz offset can be extrapolated using 30 dB/decade frequency dependence. This phase noise performance is sufficient for wireless LAN applications. When VCO operation frequency is divided by 2, the phase noise is expected to be 6 dB better [7]. Comparing with the phase noise performance of the VCO test structure and that of the VCO-divider combination, divider phase noise is sufficiently low and has almost no effect on the overall phase noise.

The VCO-divider combination measurements demonstrated a tuning range from 334 to 560 MHz, which covers the required LO2 frequency range from 350 to 550 MHz. The measured phase noise is low enough for wireless LAN application. This confirms a

VCO with a sufficiently wide tuning range and phase noise needed for the proposed receiver in Chapter 2 can be implemented in CMOS technology. If a high-frequency VCO running at a fixed frequency can be realized with low phase noise, then the phase noise and tuning range could be traded off between the high and low frequency VCO's. The high-frequency multi-band VCO is designed and demonstrated in Chapter 6.

CHAPTER 6
A LOW PHASE NOISE AND LOW POWER MULTI-BAND CMOS VCO

6.1 Introduction

CMOS voltage controlled oscillators (VCO's) have been the subject of intense studies. Despite this, high frequency MOS VCO's still remain as one of the challenging RF blocks. Especially, the higher close-in phase noise due to higher 1/f noise in CMOS continues to be a sore point. In addition, with CMOS scaling, supply voltage, V_{dd} is reduced, which limits the VCO tank voltage swing and can cause phase noise degradation. To make the matter worse, an increased demand for multi-band and multi-standard radio requires VCO's operating over a wider frequency range as we have already seen in Chapter 2. Though multiple VCO's can be used to generate signals in multiple frequency bands [56], using a single multi-band VCO is desirable to reduce area and cost [44,57].

The multi-band multi-standard VCO described in Chapter 2 runs at three fixed frequencies: 2.9, 4.8 and 5.325 GHz. To achieve sufficient performance for wireless LAN applications, its tuning range is traded for better phase noise. This chapter describe a low phase noise VCO which can support operation in four frequency bands (2.4, 2.5, 4.7, and 5 GHz) [58]. The four band operation has been accomplished by extending the use of variable L-C (VLC) tank concept [44] to 5 GHz which has been considered to be almost not possible in a 0.18-µm CMOS process and using additional switched capacitors. The low phase noise is achieved using 0.18-µm PMOS transistors with a pure SiO_2 gate oxide layer. With an 1-V power supply, phase noise at 1-MHz offset is -126 dBc/Hz and -134

dBc/Hz in the 4.7 and 2.4GHz bands. At 10-kHz offset, phase noise is -75 dBc/Hz and -85 dBc/Hz in the 4.7 and 2.4GHz bands, respectively. In addition to the reconfigurability, this circuit is the CMOS VCO with the lowest phase noise in the four frequency bands it operates. This VCO output frequencies are slightly lower than the required 2.9/4.8/5.325 GHz outputs for VCO1 in Chapter 2. But with small adjustments, it can be made suitable for the VCO1 in the proposed multi-band WLAN receiver.

To achieve low phase noise, a proper VCO topology has to be first determined. Though the wide-tuning range VCO topology in Chapter 5 can be simply adopted to implement the multi-band VCO, it has one drawback that is its bias circuit is complicated and hard to control. In reality, without careful design, the bias circuit could significantly impair VCO phase noise. A good VCO design should include the bias circuit to comprehend all noise sources. So, two single-band VCO's with bias circuits are studied before the multi-band VCO design. One is designed using all NMOS and the other using all PMOS. The phase noise performances of the all PMOS and the all NMOS VCO are compared and discussed in section 6.2. Based on the study results, a multi-band VCO circuit design is selected and described in section 6.3. The experimental results are presented in section 6.4 and conclusions are given in section 6.5.

6.2 All NMOS and PMOS VCO Comparison

For given current, NMOS transistors have smaller size than PMOS transistors to achieve the same g_m. Because of this, the VCO core using NMOS transistors can achieve a larger tuning range than its PMOS counterpart. But PMOS transistors have ~10-dB lower 1/f noise compared to that for NMOS transistors in 0.18-μm CMOS processes utilizing a pure SiO_2 gate oxide layer. PMOS transistors also have lower hot carrier induced

white noise [59,60]. Thus, PMOS VCO's can achieve better phase noise performance than NMOS VCO's [59-63]. Since the required multi-band VCO runs only at a fixed frequency in each band, its tuning range requirement is greatly relaxed, and an all PMOS VCO with lower phase noise is almost perfect for this application.

To verify this concept, an all PMOS [59-63] single-band 5-GHz VCO was implemented in a foundry 0.18-μm CMOS process. Its schematic is illustrated in Figure 6-1(a). L_1 and L_2 are formed with a single differential inductor [64] with measured inductance of 1.4nH. D_1 and D_2 are p^+ to n-well diode varactors with a measured quality factor (Q) larger than 28 at 5 GHz. M_5 and M_6 are common-source amplifiers serving as buffers to drive a measurement instrument. The loads of buffers are L-matching networks which provide output matching to 50 Ω.

The PMOS VCO exhibits an excellent phase noise at 1-V V_{dd} and 4.2-mA bias current. At 5.25 GHz, the measured phase noise is -127 dBc/Hz at 1-MHz offset frequency as shown in Figure 6-2(a). This is ~3 dB lower than the best 5-GHz MOS VCO reported to date [65]. The tuning range of the VCO is 8%.

To compare the performance of this VCO to that for an all NMOS VCO, an all NMOS VCO was also implemented in the same technology. Figure 6-1(b) shows the NMOS VCO schematic. The VCO's have the same transistor sizes and inductance. The main difference is that the p-n junction varactors of all PMOS VCO is replaced by MOS varactors (CV_1 and CV_2) with the similar capacitance. If the same p-n junction varactor is used in the NMOS VCO, the n-well nodes of p-n junction varactors have to be connected to the drain sides of VCO core in order to avoid applying control voltage higher than V_{dd}. But the n-well nodes have significant parasitic capacitance to ground with lower Q than

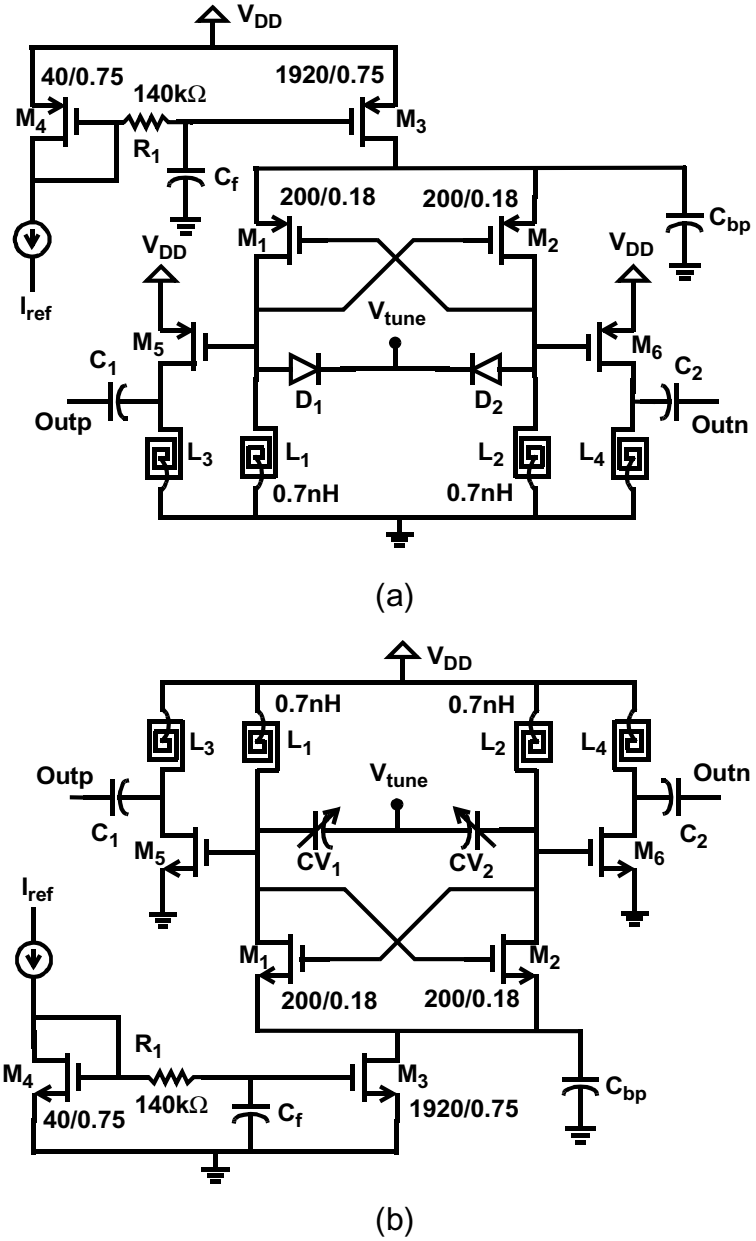


Figure 6-1 Single band 5-GHz VCO's. (a) PMOS VCO schematic, (b) NMOS VCO schematic.

the p-n varactor diodes. This would have lowered the tank Q and tuning range. The measured MOS varactor Q is 70 at 5GHz so the tank Q is limited by that for the differential inductor. At 1-V V_{dd} and 4.2-mA bias current, the NMOS VCO phase noise is ~9 dB worse than that for the PMOS VCO for offset frequencies ranging from 10 kHz to 10 MHz

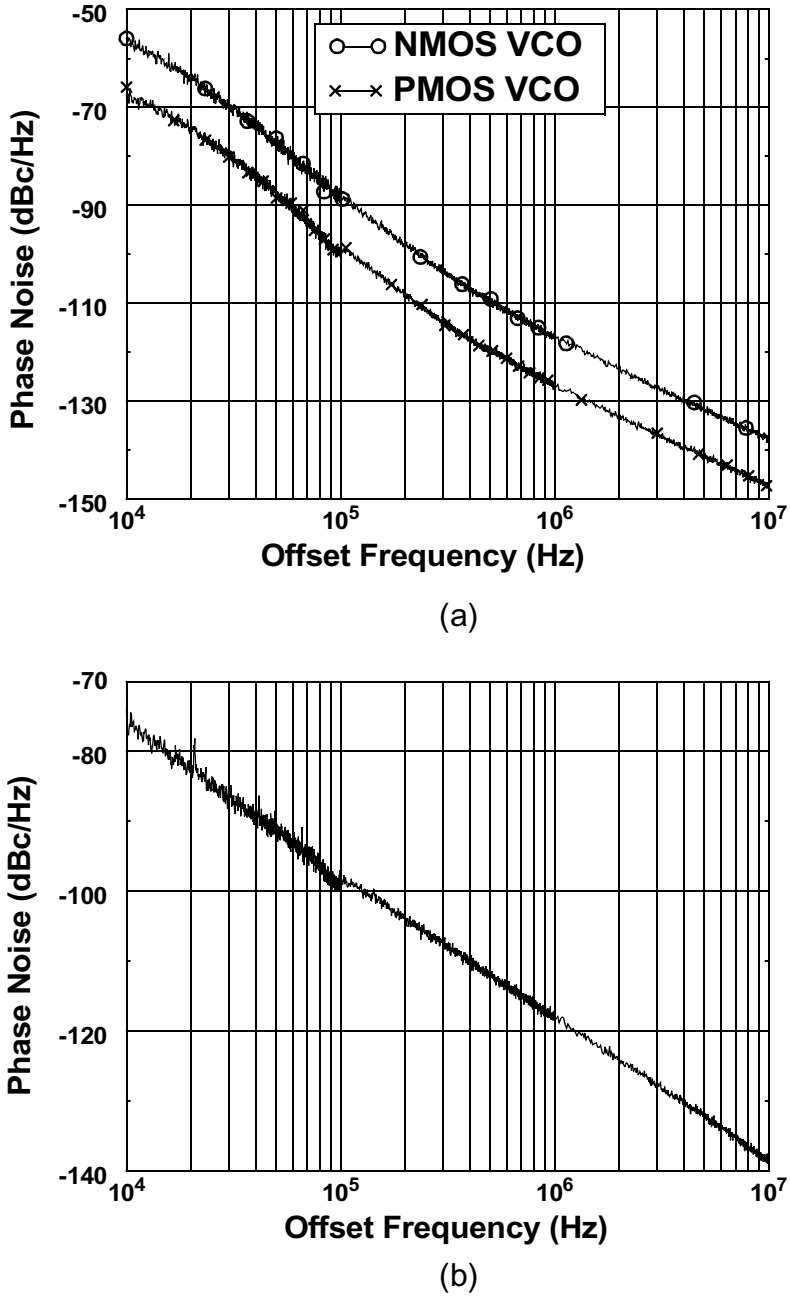


Figure 6-2 Measured phase noises of single-band 5-GHz VCO's. (a) NMOS and PMOS VCO phase noise at 1-V V_{dd} and 4.2-mA current, (b) PMOS VCO phase noise at 0.66-V V_{dd} and 1.8-mA current.

as shown in Figure 6-2(a). Due to the large tunability of MOS varactor, the NMOS VCO achieves a 15% tuning range. The larger tuning range degrades NMOS VCO phase noise. In the worst case, if all VCO noise comes from the control path, when the VCO gain is

doubled, the phase noise will increase by 6-dB. So the tuning range difference between NMOS and PMOS VCO's can not account for all the 9-dB phase noise difference. The PMOS VCO has better phase noise.

Another interesting characteristic of the PMOS VCO in this design is that it exhibits superior close-in phase noise when it runs at low power consumption. The VCO could oscillate under only 0.66-V V_{dd}. When the VCO bias current is reduced to ~ 2 mA, the flicker noise decreases and the VCO displays almost perfect -20-dB/decade phase noise slope down to 10-kHz offset frequency. At 0.66-V V_{dd} and 1.8 mA bias current, or 1.2-mW power consumption, -76 dBc/Hz phase noise is obtained at 10 kHz offset from 5.3 GHz carrier as shown in Figure 6-2(b). The measured phase noise at 1 MHz offset is -118 dBc/Hz. Achieving these at the 1.2-mW power consumption is particularly exciting. The -76 dBc/Hz at 10 kHz offset is ~ 6 dB lower while the -118 dBc/Hz at 1 MHz offset is ~ 9 dB higher than those at V_{dd} = 1V and bias current of 4.2 mA. These indicate that the bias current can be controlled to balance the close-in phase noise and phase noise at higher frequency offsets. Comparing to a complementary cross-coupled VCO topology, the PMOS VCO topology has a larger head room. So, it is better suited for low V_{dd}, low power and low phase noise applications. Based on this, the all PMOS circuit topology is chosen for the multi-band VCO implementation.

6.3 Multi-Band VCO

6.3.1 Multi-Band VCO Circuits Design

The multi-band VCO schematic is given in Figure 6-3. M_1 and M_2 form the VCO core. M_3 and M_4 form a PMOS current mirror. A 20-pF on-chip bypass cap C_{bp} is placed at the VCO core virtual ground node to suppress the noise around $2\omega_0$ and higher. The

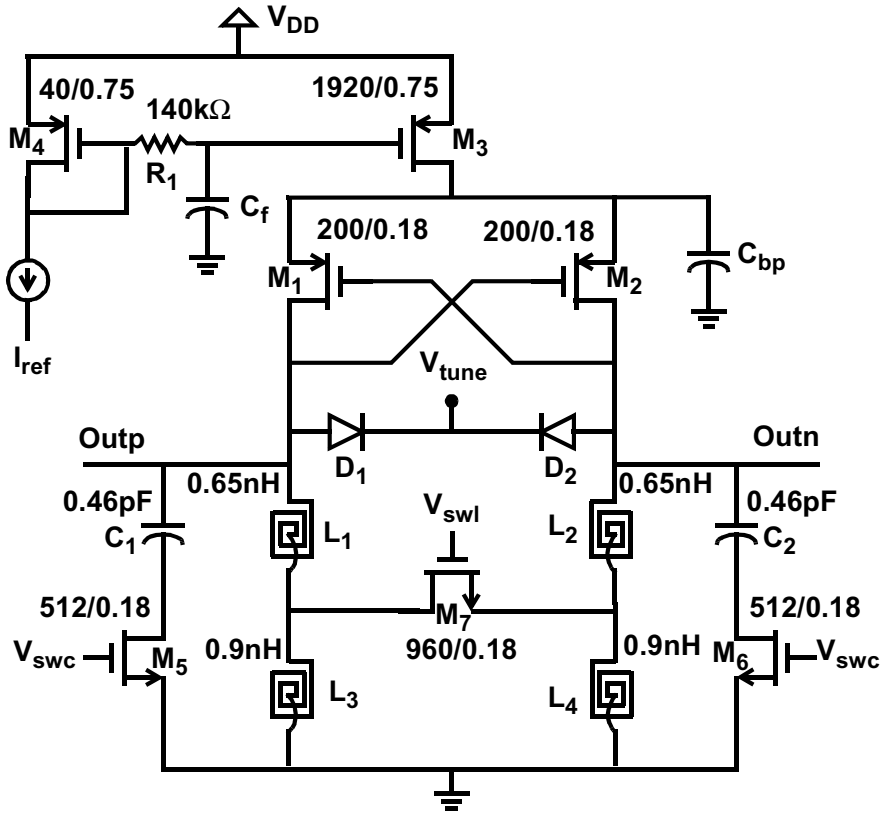


Figure 6-3 A schematic of the multi-band VCO

length and width of M_3 are made large (0.75, 1920 μm) to reduce 1/f noise, thus close-in phase noise. The 1/f noise from M_4 is amplified by M_3 and can also degrade phase noise. Besides reducing I_{ref} to ~100 μA to lower 1/f noise, a 140-kΩ on-chip resistor and an on-chip capacitor (C_f) are inserted between M_3 and M_4 gates to further attenuate 1/f noise. The bias circuitry and VCO core transistors in multi-band VCO are identical to those of the single-band PMOS VCO in Fig. 2(a). Although, not shown, the VCO outputs are buffered by on-chip LC tuned buffers which are similar to the buffers shown in Figure 6-1(a).

The diode varactors D_1 and D_2 (p-n junction) are used for fine tuning. Though in each band, only one fixed output frequency is required by the system, the fine tuning is used to compensate process variations and modeling inaccuracies. The p^+ to n-well diode

varactors in the multi-band VCO and single-band PMOS VCO have the same layout geometry thus the Q. The varactor tunability is defined by the ratio of the maximum capacitance over the minimum capacitance. The measured tunability of p^+-to-n-well diode varactor is 1.34 when the reverse biased voltage changes from 0 to 1.8 V.

The unique feature of multi-band VCO is its tank. The multi-band operation is realized by using a combination of inductor [44,45,66] and capacitor switching [49,63]. As shown in Figure 6-3, the differential inductors L_1 to L_4 and M_7 form the switched inductors/variable L-C tanks [44,45,66], and capacitors C_1 and C_2 in combination with M_5 and M_6 form switched capacitors.

The switched components coarsely tune VCO to the four operation bands: 2.4, 2.5, 4.7 and 5 GHz. Two control voltages V_{swl} and V_{swc} are used to select the bands. When V_{swl} is high, M_7 is on and shorts out L_3 and L_4, and when V_{swc} is high, M_5 and M_6 are on, and C_1 and C_2 are added to the L-C tank. When L_3 and L_4 are shorted out, the parasitic capacitances of the structures are also shorted out, and this leads to additional capacitance switching. The equivalent circuits models when V_{swl}=V_{swc}=0V and when V_{swl}=V_{swc}=1.8V are shown in Figures 6-4(a) and (b), respectively.

The utilization of both capacitor and inductor switching enables use of smaller varactors for fine tuning in each band compared to those in a wide tuning range VCO using only varactors [57]. This lowers the required VCO gain and phase noise. The capacitor switching occupies a smaller area, but is more suitable for small frequency changes. Additionally, when the switched frequency range is large, e.g. 2.5 to 5GHz, the inductor-capacitor switching results in lower power consumption and phase noise [44] compared to the capacitor only switching case.

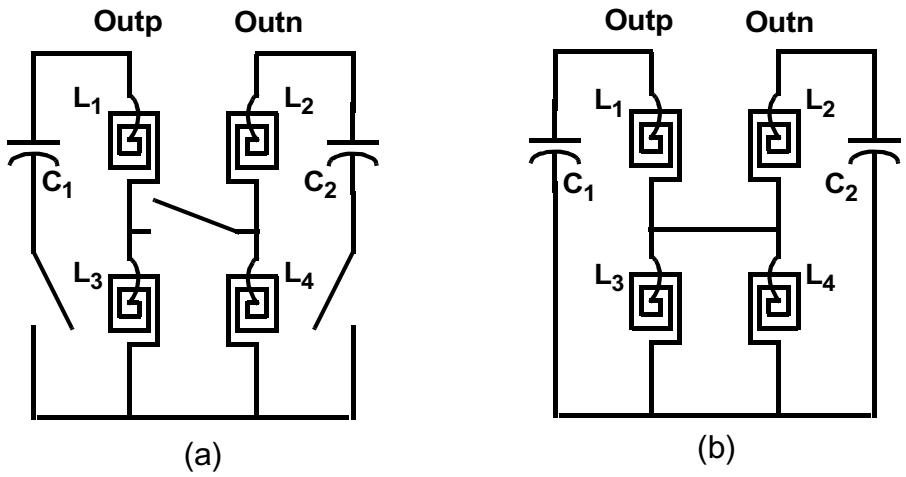


Figure 6-4 Equivalent circuit models at (a) V_{swc}=V_{swl}=0V, and (b) V_{swc}=V_{swl}=1.8V

But the switched components could have degraded Q due to additional series resistance. When the switching transistors are off, the parasitics associated with the transistors could also degrade the switched inductor/capacitor Q. The switched components have to be carefully designed and laid out to maintain comparable performance to that of the single-band PMOS VCO.

6.3.2 Switched Capacitor

The capacitors, C_1 and C_2 in the switched capacitors are inter-digital metal-to-metal capacitors [67]. A simple horizontal bar structure [67] is fabricated using only the metal 5 layer as shown in Figure 6-5(a). The width of metal bar and space between the bars are the minimum dimensions allowed in the process. Both are 0.28 μm. The measured Q is 130 at 2.4 GHz and 62 at 5 GHz. The actual Q is expected to be higher than the measured because the Q extraction procedure does not exclude the probe-pad contact resistance [68]. The measured series resistance of the 255 fF metal-to-metal capacitor is ~ 2 Ω where the total contact resistance could be as high as 1.2 Ω [67]. The area of

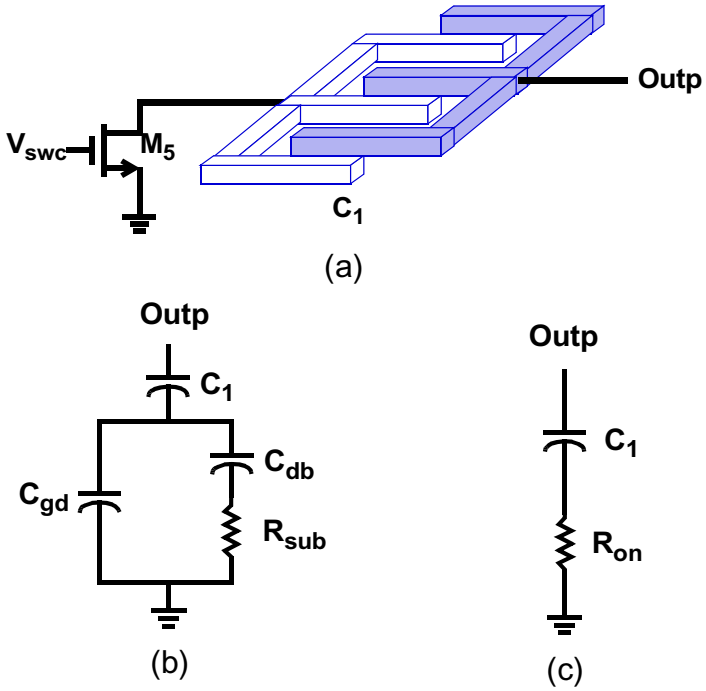


Figure 6-5 The Switched capacitor. (a) A illustration, and its circuit model (b) when the switch is off, (c) when the switch is on.

for a 255 fF metal capacitor is ~ 54 x 27 μm^2 so the capacitance density is ~ 0.17 $fF/\mu m^2$. If more metal layers are used to build this type of capacitor, the capacitance density is comparable to the density of metal-insulator-metal (MiM) cap (~1 $fF/\mu m^2$ in 0.18-µm CMOS process).

As illustrated in Figure 6-5(b), when M_5 is off, the parasitic capacitance C_{db} and C_{gd} of the transistor are in series with C_1. Here C_{db} is the drain-to-substrate capacitor and C_{gd} is the drain-to-gate capacitor. The V_{swc} node is virtual ground due to the differential VCO topology. The transistor drain-to-substrate resistor R_{sub} is in series with C_{db} and degrades the switched capacitor Q. To minimize the loss through R_{sub}, the switch layout is broken into several cells and each cell is surrounded with a 7-µm wide guard ring. In order to increase tunability, C_{db} and C_{gd} should be made smaller thus it requires smaller M_5

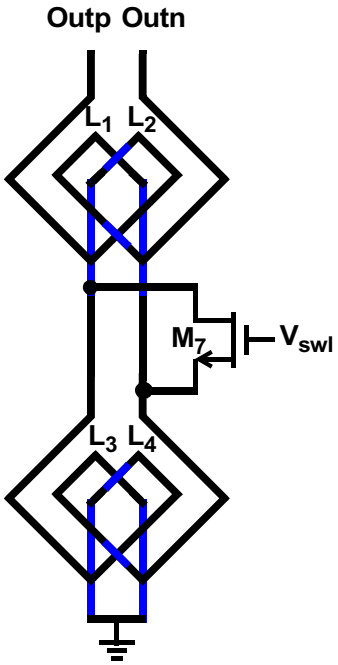


Figure 6-6 The switched inductor.

width. But, the transistor cannot be made arbitrarily narrow, since its finite on-resistance, R_{on}, increases the tank loss in its on-state (Figure 6-5(c)).

The switch size is 512/0.18μm as shown in Figure 6-4. With this, the switched capacitor achieves almost the same measured Q factors when V_{swc} is 0 and 1.8 V. The Q factors are ~ 55 and ~ 25 at 2.4 and 5 GHz, respectively. The measured tunability is 1.6 for the switched capacitors.

6.3.3 Switched Inductor

The layout of the switched inductor is shown in Figure 6-6. Two differential inductors physically realize L_1/L_2 and L_3/L_4. In order to lower magnetic coupling between the two differential inductors, they are placed with 45° rotation as shown in Figure 6-6. The inductors use metal 4, 5, 6 layers shunted to lower series resistance. A polysilicon ground shield is placed underneath the inductors. The switch M_7, when turned on becomes virtual ground and shorts out L_3 and L_4. When the switch is on, it adds series resistance to the

Table 6-1 Multi-band VCO Performance Summary

	Band 1	Band 2	Band 3	Band 4
V_{swl} (V)	0	0	1.8	1.8
V_{swc} (V)	1.8	0	1.8	0
V_{tune} (V)	0 – 3.0	0 – 3.0	0 – 3.0	0 – 3.0
Tuning Range (GHz)	2.40 – 2.44	2.47 – 2.52	4.65 – 4.80	4.92 – 5.12
Measurement Frequency (GHz)	2.42	2.51	4.72	5.01
Phase Noise (dBc/Hz) at 10 kHz	-85	-82	-75	-73
Phase Noise (dBc/Hz) at 100 kHz	-112	-110	-104	-103
Phase Noise (dBc/Hz) at 1 MHz	-134	-132	-126	-125
RMS Jitter from 10kHz - 10MHz (degree)	0.36	0.51	1.0	1.4
V_{DD} (V)	1	1	1	1
I_{VDD} (mA)	4.6	4.6	6	6
FOM at 1-MHz Offset Frequency	-195	-193	-192	-192

inductor and degrades the inductor Q. Placing the switch between the differential nodes [66] reduces the M_7 size by a half for the same Q degradation compared to that of the single-ended switched inductor arrangements in [44] and [45]. This in turn reduces the unwanted parasitics associated with M_7 when it is off. When Vs_{wl}=0V, the measured quality factor Q (Q_{ps}) based on the phase stability factor [69] is about 5 at 2.4 GHz. When V_{swl}=1.8V, the measured Q_{ps} is ~6 at 5GHz.

6.4 Multi-Band VCO Experimental Results

The circuit was fabricated on 10-Ω-cm p-substrates. The VCO has been tested on an FR-4 PC Board using an HP E5500 Frequency Discriminator. The performance is summarized in Table 6-1. Two low bands are tuned to around 2.4 and 2.5 GHz. With 1-V V_{dd} and 4.6mA bias current, phase noise is -134dBc/Hz at 1-MHz offset from the 2.42-GHz carrier. This is ~5 dB better than that of the other CMOS VCO's operating in the 2-3 GHz

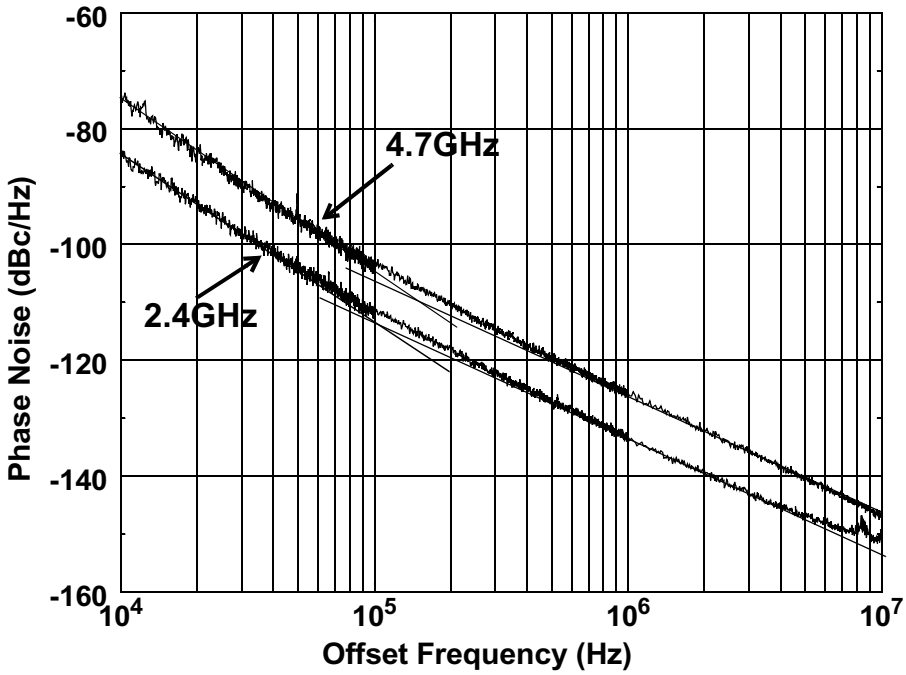


Figure 6-7 Measured multi-band VCO phase noise at 4.7 GHz and 2.4 GHz, at 1-V V_{dd}, and 6 and 4.6 mA bias current, respectively.

range [70]. At 10-kHz offset, phase noise is -85dBc/Hz, which is sufficient for 802.11b applications.

The two high bands are near 4.7 and 5GHz. At 4.7GHz, it achieves phase noise of -126 dBc/Hz at 1-MHz offset with 1-V V_{dd} and 6mA bias current. This phase noise performance is one of the lowest reported to date for CMOS VCO's operating near 5 GHz, and is 10dB better than [57] which is designed for multi-band operation. At the same bias condition, the VCO has phase noise of -125dBc/Hz at 1-MHz offset in the 5GHz band. The phase noise data for the 2.4 and 4.7 GHz are plotted in Figure 6-7. The corner frequencies are around 100 kHz for the two bands.

RMS jitter measures integrated phase noise and is an important VCO specification. RMS jitter at the VCO output is related to phase noise by [54,71]

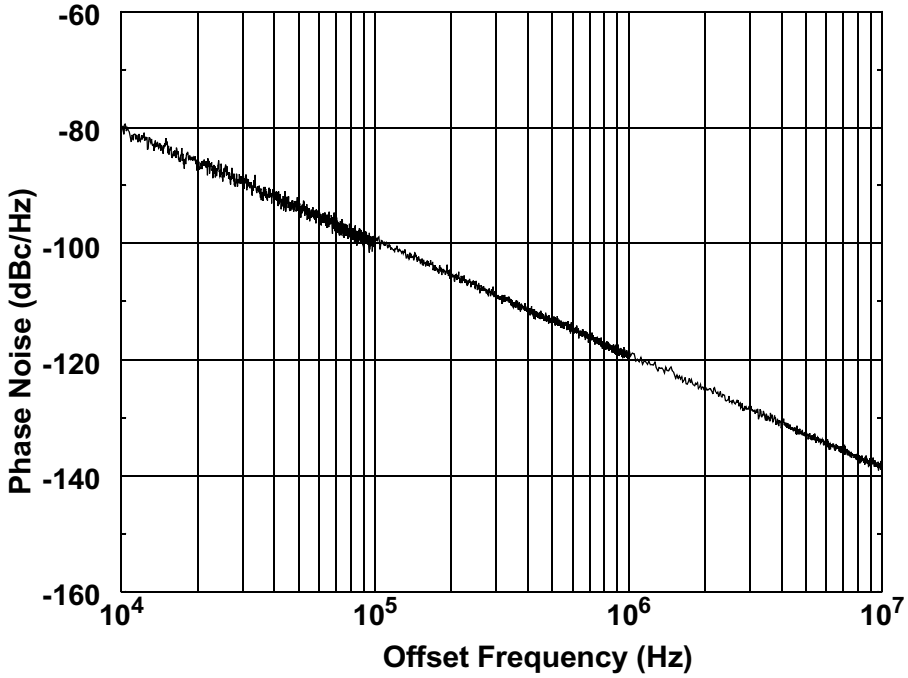


Figure 6-8 Measured multi-band VCO phase noise at 4.7 GHz at 0.8-V V_{dd} and 2.5-mA current.

$$Jitter = \frac{180}{\pi} \cdot \sqrt{2 \cdot \int_{f_1}^{f_2} S_{\phi}(f)\,df} \tag{6.1}$$

Here S_{ϕ} is the output phase noise power spectral density and f_1-f_2 is the interested frequency range. The measured RMS jitter is sufficiently low. From 10 kHz to 10 MHz, it is 0.36, 0.51, 1.0 and 1.4 degree for the 2.4, 2.5, 4.7 and 5.15-GHz band, respectively.

As explained in the multi-band system, the VCO is intentionally designed with smaller VCO gain or a smaller tuning range to achieve lower phase noise. The tuning ranges in the 2.4 and 5 GHz bands are 40 and 200 MHz.

At 4.7 and 5-GHz bands, this multi-band VCO exhibits low close-in phase noise at low power consumption as the single-band PMOS VCO. The multi-band VCO starts to oscillate at 0.7-V V_{dd} and 1.7 mA current. At 4.7 GHz, excellent phase noise is obtained at 0.8-V V_{dd} and 2.5-mA current, or 2-mW power consumption as illustrated in Figure 6-8.

The measured phase noise at 10 kHz offset is -80 dBc/Hz. This is the best close-in phase noise that has been measured near 5-GHz using integrated CMOS VCO's. The measurements suggest that close-in phase noise can be improved at the expense of degraded phase noise at higher offset frequencies by decreasing the bias current. The phase noise slope is -20dB/decade and RMS jitter from 10 kHz to 10 MHz is 0.81 degree.

A widely used figure of merit (FOM) for VCO's is defined as

$$FOM = L\{f_{offset}\} - 20\log\left(\frac{f_0}{f_{offset}}\right) + 10\log\left(\frac{P_{DC}}{1mW}\right) \tag{6.2}$$

Here, $L\{f_{offset}\}$ is the measured phase noise at offset frequency f_{offet} from the carrier frequency f_0. P_{DC} is VCO power consumption in mW. The best measured FOM for the VCO is -195 dBc/Hz in the 2.4GHz band, which is excellent. The low phase noise and FOM are pleasant surprises for oscillators utilizing variable L-C tanks. The required reduction of inductance for 5-GHz operation (0.65 nH) has been expected to make the tank Q degradation due to the loss of switching transistor, M_7 significantly greater than at lower frequencies. Because of this, use of switched L-C tanks utilizing 0.18-μm MOS transistor switches for 5-GHz oscillators has been considered to be impractical. Comparing with the single-band 5GHz VCO performance, to achieve the similar phase noise at 1MHz offset, the multi-band VCO needs to consume ~1.8-mA more current. The results reported in this paper demonstrated that it is not only possible to use switched LC tanks for 5 GHz operation but excellent performance can be attained.

A die photograph of the VCO is shown in Figure 6-9. The chip size is 0.8 x 0.8 mm^2. The chip size excluding the bond pads is 0.36 mm^2. This should be around ~25%

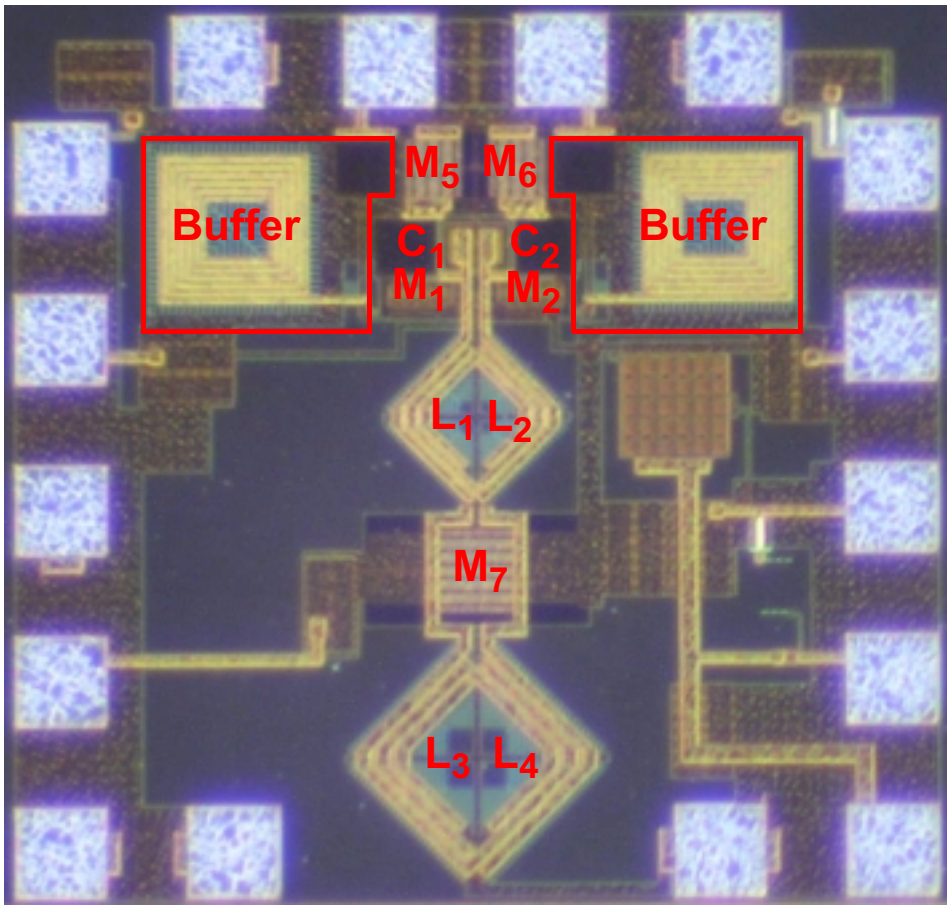


Figure 6-9 Multi-band VCO die photograph. The chip size is 0.8 x 0.8 mm^2

smaller than the area that would have been occupied by two separate VCO's operating near 2.4 and 5.2GHz.

6.5 Conclusion

A four-band (2.4, 2.5, 4.7, and 5.0 GHz) 0.18-μm all PMOS VCO operating with an 1-V power supply is presented. VCO output frequencies are close to the required frequencies by proposed multi-band WLAN receiver. By reducing the inductance and/or capacitance of VCO tank, this VCO can be used as VCO1 in the multi-band receiver. Excellent VCO phase noise performance is obtained from this VCO, which is credit to the all PMOS VCO topology and low VCO gain. Superior close-in phase noise is also

obtained at only 2mW power consumption. These phase noise performances are sufficient for WLAN applications. These results demonstrate that by using PMOS transistors in a 0.18-μm CMOS process with a pure SiO_2 gate oxide layer and inductor-capacitor switching, a low voltage multiple-band VCO operating up to 5 GHz with excellent phase noise performance can be implemented.

The successful demonstration of the multi-band VCO with the low phase noise strongly supports the design concept of the multi-band receiver. Tuning range and phase noise of VCO1 and VCO2 can traded off. It also illustrates that the CMOS technology can be used to implement the multi-band operation with reduced area and cost. The next step is to investigate whether it is possible to implement the multi-band LNA and mixer by using CMOS technology required in the proposed multi-band receiver. This is discussed in the next Chapter (Chapter 7).

CHAPTER 7
MULTI-BAND CMOS RF/IF DOWN-CONVERTER

7.1 Introduction

A Low Noise Amplifier (LNA) is a critical circuit in a receiver chain. With adequate gain for the LNA, the total receiver noise figure is set by the noise figure of the LNA and blocks preceding the LNA. Because of this, the amplifier has to be low noise as its name indicates. CMOS LNA's received much attention. But when this project started, implementing a 5-GHz CMOS LNA was considered as a challenge. And, even worse, to compete with the other technology (SiGe bipolar and GaAs), the noise figure of CMOS LNA should be less than 3 dB at low power consumption of less than 10 mW [72]. To address this issue, a feasibility study was first carried out by implementing a single band 5-GHz LNA.

A 5-GHz single band LNA is discussed in section 7.2. With 10 mW power consumption and noise figure of 2.16 dB at 5.25 GHz, it is one of the best 5-GHz CMOS LNA's reported to date [72]-[75]. Overall, the 5-GHz LNA is sufficient for wireless LAN applications. The second part of the feasibility study is to develop a multi-band CMOS LNA and mixer working at 2.4 GHz and 5.15 GHz. The LNA working with a down-conversion mixer forms an RF/IF down-converter. In section 7.3, a dual-band RF/IF down-converter fabricated in a 0.18-μm CMOS technology is presented. With the switched resonators used in the wide tuning range VCO, this dual-band down-converter

can be switched between the 2.4 and 5.15 GHz operation modes. The switched gain control is also incorporated to relax the linearity requirement.

7.2 5-GHz Single Band Low Noise Amplifier

A differential LNA [76] is commonly employed in WLAN transceiver design to reduce the packaging sensitivity and second order distortion. This, in addition to doubling the LNA power consumption compared to a single-ended LNA, requires an off-chip balun with finite loss to convert the single ended signal from an antenna to balanced/differential signal. This increases the component count and noise figure of the receiver [11]. A single-ended circuit, on the other hand, is more sensitive to the package parasitics. The packaging bondwire inductance could significantly degrade LNA power gain as well as noise performance. A 5-GHz single-ended LNA with good noise figure has been reported [72], but it requires thinning the substrate to 20 μm, and it is measured on-wafer without including the packaging effects. Additionally, the IP_2 performance of single ended LNA's has not been widely discussed in the literature. To address all these issues, a single-ended 5-GHz LNA for UNII and HIPERLAN/2 band between 5.15 and 5.35 GHz has been fabricated and tested on a printed circuit board (PCB) [77].

7.2.1 5-GHz LNA Circuit Design

The 5-GHz LNA employes a commonly used cascode common-source topology [78-80]. Its simplified schematic is illustrated in Figure 7-1(a), where the parasitics from the package are omitted for clearer illustration.

L_{pcb} is an off-chip inductor along with the packaging bondwire inductance, which tunes the LNA input to the desired band. L_s provides the real part to input impedance for matching. M_2 is a common-gate transistor. The LNA output matching uses an on-chip

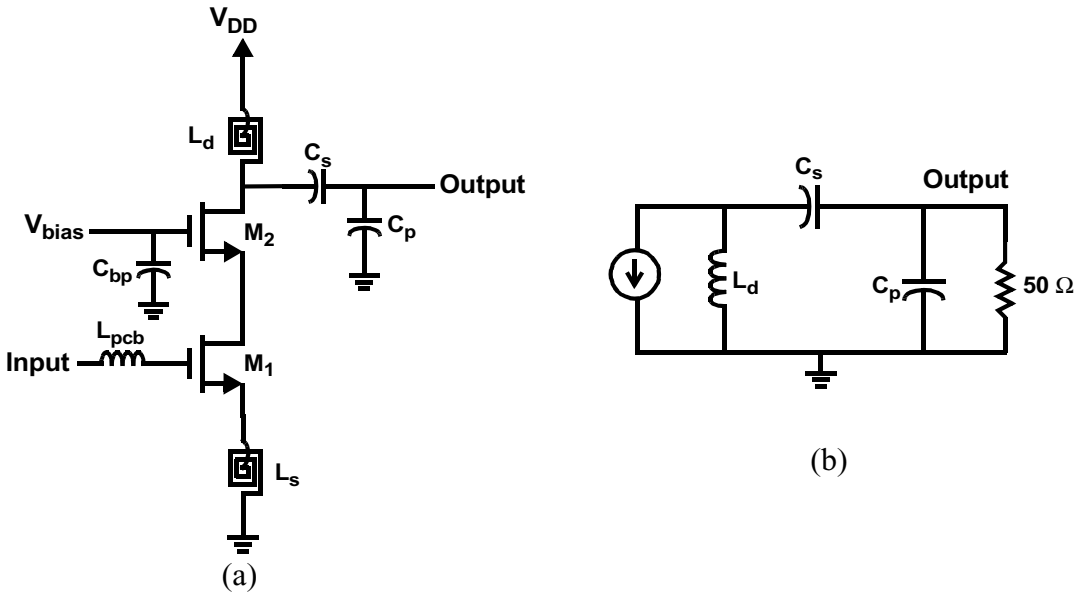


Figure 7-1 A 5-GHz Low Noise Amplifier (LNA). (a) A schematic of it, and (b) LNA output tank acts as band-pass filter.

inductor, L_d and a capacitive transformer [54-55, 79-82] which includes C_s and C_p. C_s and C_p are metal-to-metal capacitors. The top plate is formed with metal 4 and 6 layers while the bottom plate is formed with metal 3 and 5 layers. The parasitic inductance and capacitance from the package are modeled and reflected in the LNA design. To reduce the inductance between on-chip ground and board ground, nine down-bondwires are used in parallel. The chip die photo is shown in Figure 7-2. The area is 830 x 830 μm^2.

The one design issue worth mentioning here is the LNA linearity. The LAN output can be expressed as [7]

$$y(t) = \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t), \qquad (7.1)$$

here *y(t)* is the LNA output and *x(t)* is the input. α_1, α_2 and α_3 are gains for fundamental, second order products and third order products, respectively. Then, the input voltage corresponding to the third order intercept point (IP3) can be expressed by [7]

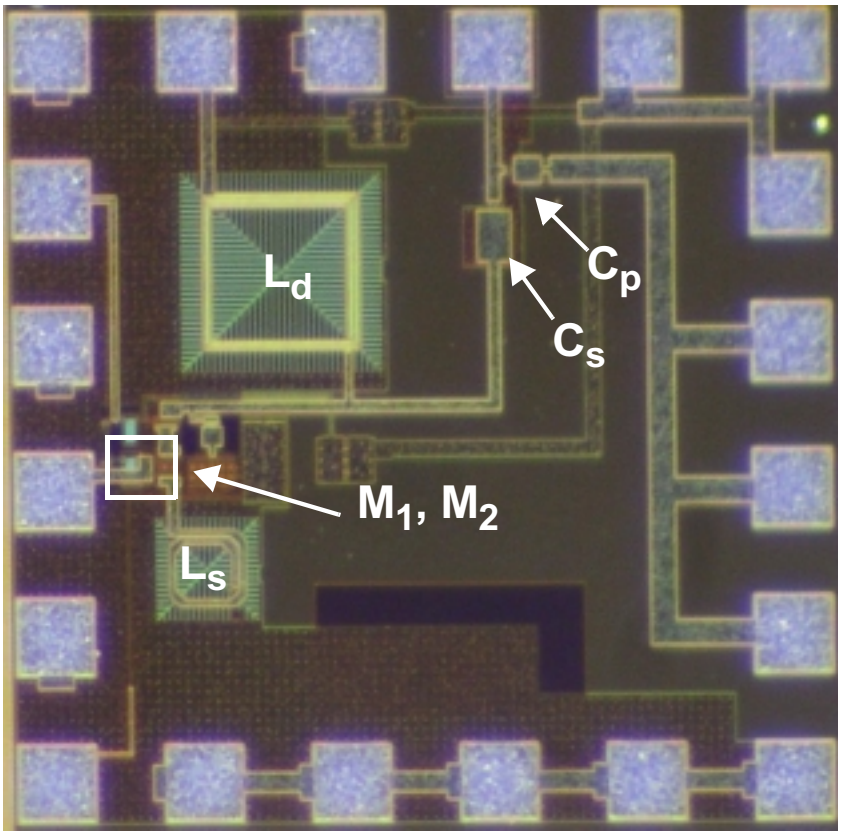


Figure 7-2 A 5-GHz LNA die photo. The area is 830 x 803 μm^2.

$$A_{IP3} = \sqrt{\frac{4}{3}\left|\frac{\alpha_1}{\alpha_3}\right|}. \tag{7.2}$$

Here A_{IP3} is the amplitude in vol. Using a similar approach, A_{IP2} can be found to be

$$A_{IP2} = \frac{\alpha_1}{\alpha_2}. \tag{7.3}$$

The amplitude of second and third order products are determined by their corresponding gain, α_2 and α_3. The third-order intermodulation products (IM3) have frequencies close to the fundamental, thus tuned output matching networks have little effects on α_3. The A_{IP3} is mainly determined by the transistor linearity and input matching network [55].

But A_{IP2} is quite different. The second-order intermodulation products (IM2) are either close to DC or 2 times the fundamental. The frequencies of IM2 is far away from the output tank tuned frequency. The LNA output tank acts like a band-pass filter as illustrated in Figure 7-1(b). Low frequency part of IM2 is shunted to ground by L_d and the high frequency part by C_p. Since the capacitive output matching network attenuates α_2, A_{IP2} is not only determined by the transistor linearity and input matching network. With this LNA topology, a good A_{IP2} is expected because the output tank will keep α_2 small (Eq. (7.3)). In a receiver chain, high frequency spurs will be filtered out by the low pass filter after the last down-conversion, so the low frequency part of IM2 could be more problematic through finite mixer RF-to-IF feedthrough, and should receive more attention [11].

7.2.2 5-GHz LNA Experimental Results

The LNA was fabricated in a 0.18μm foundry CMOS process. The Chip-On-Board (COB) packaging technique is used for circuit characterization. The measured LNA characteristics are summarized in Table 7-1. The initial measurements showed that the LNA output is tuned around 4.5 GHz. To correct this problem, an off-chip shunt capacitor (2.2pF) was placed at the output to re-tune the LNA. The measured LNA S-parameters are illustrated in Figure 7-3. Over the entire 5.15-5.35 GHz band, $|S_{11}|$ and $|S_{22}|$ are less than -10 dB. The measured gain and noise figure (NF) are shown in Figure 7-4. The LNA has maximum transducer power gain of 16.1 dB and minimum reverse isolation of 21 dB at 5.25 GHz, while the measured LNA noise figure (NF) is 2.16 dB. At power consumption of 10 mW, the measured noise figure is the same as that in Chiu and Lu [72], and the gain is 5-dB higher than that in Chiu and Lu [72]. Additionally,

Table 7-1 Measured performance summary of 5-GHz LNA

Frequency (GHz)	5.15	5.25	5.35
V_{dd} (V)	1.8	1.8	1.8
Current (mA)	5.8	5.8	5.8
S_{11} (dB)	-11.1	-15.9	-26.3
S_{22} (dB)	-10.0	-14.8	-24.6
S_{21} (dB)	15.5	16.1	15.4
S_{12} (dB)	-22.9	-21	-22.8
Noise Figure (dB)	2.0	2.16	2.3
Input P_{1dB} (dBm)	-13.6		
P_{1dB} (dBm)	1.5		
Input IP_3 (dBm)	-4.3		
IP_3 (dBm)	11.8		
Input IP_2 (dBm)	>64 (20 MHz IP)		
Input IP_2 (dBm)	47 (10.42 GHz IP)		

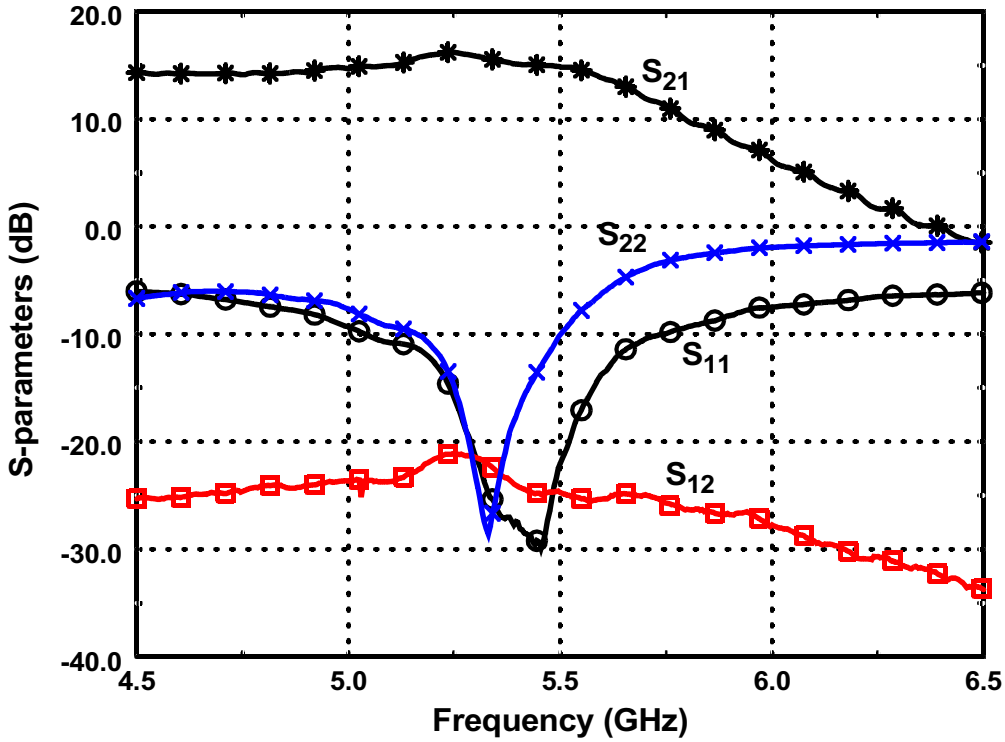


Figure 7-3 Measured 5-GHz LNA S-parameters

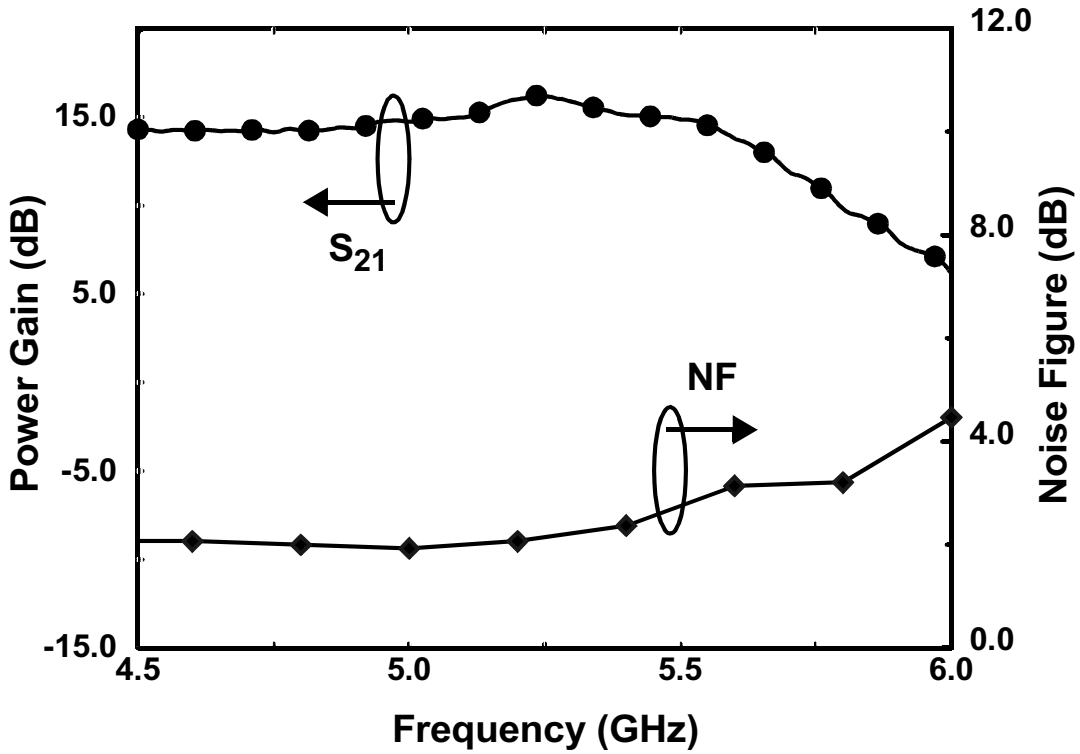


Figure 7-4 Measured 5-GHz LNA gain and noise figures.

the LNA in Chiu and Lu [72] requires a special substrate thinning step to achieve the low noise figure. More importantly, unlike in Chiu and Lu [72], the LNA in this paper is measured on a PC board.

LNA input 1-dB gain compression point (IP_{1dB}) has been tested by applying a single-tone 5.25-GHz sinusoid signal. The measured input P_{1dB} is -13.6 dBm and P_{1dB} is 1.6 dBm as shown in Figure 7-5.

The LNA linearity was characterized using a two-tone test. Input frequencies are 5.2 GHz and 5.22 GHz. The third-order intermodulation products are at 5.18 GHz and 5.24 GHz. The measured LNA input IP_3 is -4.3 dBm as illustrated in Figure 7-6. The IP3 is 11.9 dBm.

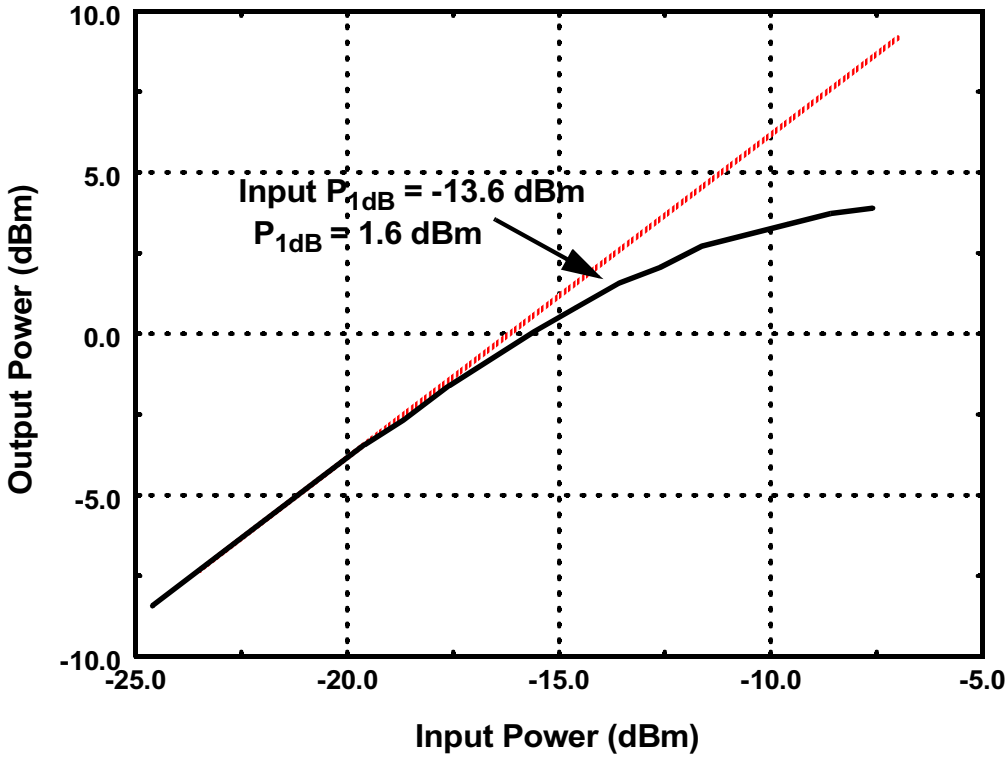


Figure 7-5 Measured 5-GHz LNA 1-dB gain compression point.

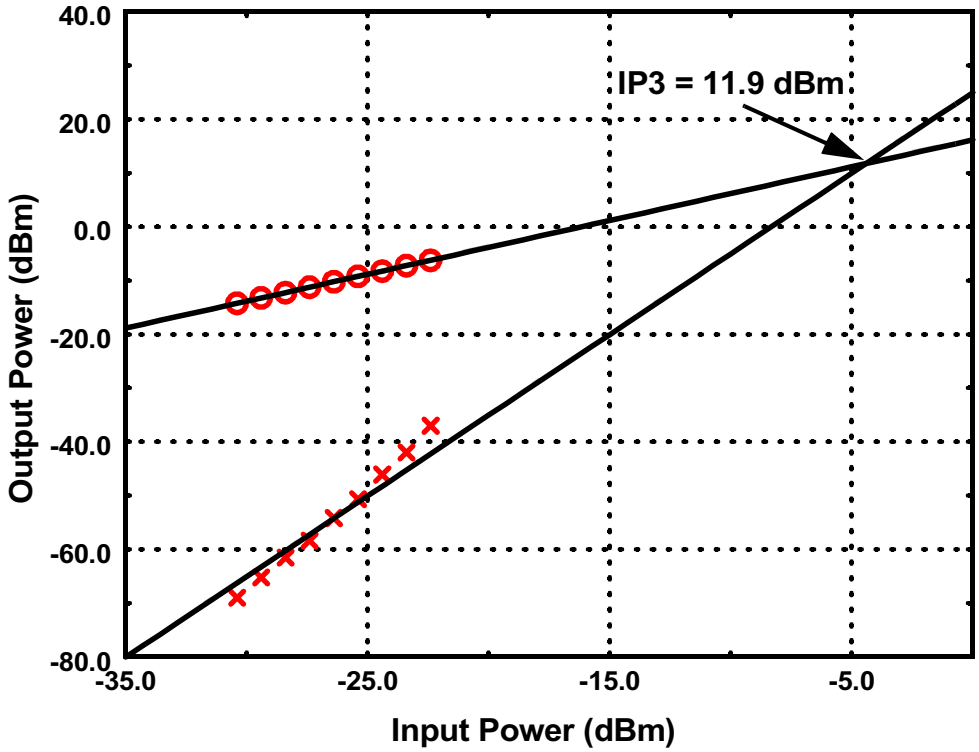


Figure 7-6 Measured 5-GHz LNA third-order intercept point.

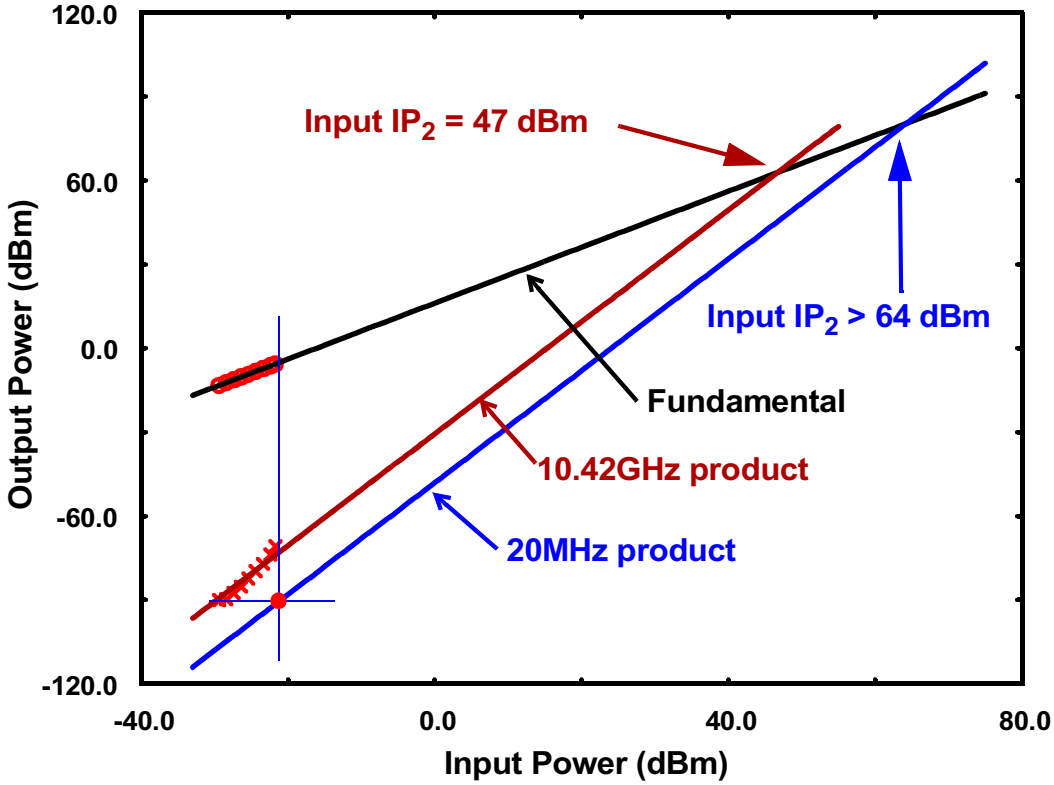


Figure 7-7 Measured 5-GHz LNA second intercept point (IP_2). The input IP_2 is greater than 64 dBm using 20-MHz intermodulation product.

The second-order intermodulation products are at 20 MHz and 10.42 GHz. The second-order intermodulation product (IP) at 20 MHz, which is the relevant product for characterizing LNA's for direct conversion or low IF radios, could not be detected for the maximum input power level of ~-21dBm. The lower bound of IP_2 is estimated by assuming that the intermodulation product power level is equal to the noise floor of -90 dBm. The estimated input IP_2 is greater than 64 dBm as shown in Figure 7-7. The IP_2 estimated using the 10.42 GHz product is also plotted in Figure 7-7. The input IP_2 is 47 dBm. These are high and adequate even for direct conversion WLAN radios [76,83,84]. These high IP_2's are due to the filtering action of LNA output matching network. The second order IP at 20 MHz is about 8 octaves away from the 5.2 GHz fundamental frequency and is greatly attenuated by the filter action.

From the single-band 5-GHz LNA measurement results, clearly, it shows sufficient performance for wireless LAN applications. This LNA is suitable for lower UNII and HIPERLAN/2 sub-band. CMOS technology can be used to implement a 5-GHz low noise amplifier.

7.3 Dual-band CMOS RF/IF Down Converter with Gain Control

A 5-GHz LNA presented in the last section works in only one band. In this section, a dual-band RF/IF down converter operating at 2.4 and 5.15 GHz fabricated in a 0.18-μm foundry CMOS process is presented [85].

The RF/IF down converter is composed of a single set of RF block. Comparing with a radio having two sets of RF block [86-88], this implementation saves area thus cost. A dual-band low noise amplifier (LNA) with two inputs is tuned to the two resonant frequencies by controlling the voltage on a switched resonator [44,45]. The same switched resonator is also used to switch the LNA between the high gain and low gain modes. Frequency tuning using only capacitors leads to unnecessarily large power consumption especially at lower frequency bands. Switched resonators in which both capacitance and inductance are simultaneously tuned can provide a better balance between inductance and capacitance at all frequency bands. This should lead to a better trade-off between power consumption and gain.

The circuit is designed to operate around 2.4 and 5.15 GHz. At 2.4 GHz, the circuit draws 14 mA from a 1.8V supply and has 39.8-dB voltage gain, 1.5-dB double side band (DSB) noise figure (NF) and -12.7-dBm input referred IP3 (IIP3). At 5.15 GHz, the circuit draws 23 mA, and shows 29.2-dB voltage gain, 4.1-dB DSB NF and -4.1-dBm IIP3. By setting the matching network between the LNA output and mixer input for 2.4-GHz oper-

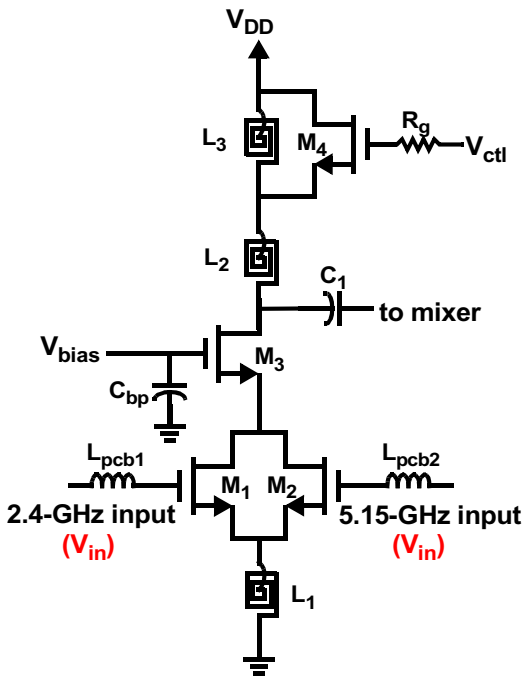


Figure 7-8 A schematic of dual-band Low Noise Amplifier

ation, when the down-converter is set to operate in the 5.15 GHz band, a low gain mode needed to improve the overall dynamic range of a receiver is realized. Reversing the roles, a low gain mode for the 2.4 GHz band is also implemented. The voltage gain is about 22 dB at both bands in the low gain mode.

7.3.1 Dual-Band RF/IF Down Converter Circuit Design

Figure 7-8 shows a dual-band LNA schematic. Once again, the bondwire inductance is not shown. M_1 and M_2 are input transistors. M_1 is for the 2.4 GHz band input and M_2 is for the 5.15 GHz input. When the LNA works in one band, the operation in the second band is disabled by turning the second transistor off. For example, when the LNA receives 2.4 GHz signals, M_2 is off, thus all the LNA current goes through M_3 and M_1. M_1 and M_3 form a cascode amplifier. L_1 is a source degeneration inductor. When M_2 amplifies 5.15 GHz signals, M_1 is turned off. L_{pcb1} and L_{pcb2} are off-chip inductors for input matching. The gate of M_3 is ac grounded through an on-chip bypass capacitor C_{bp}.

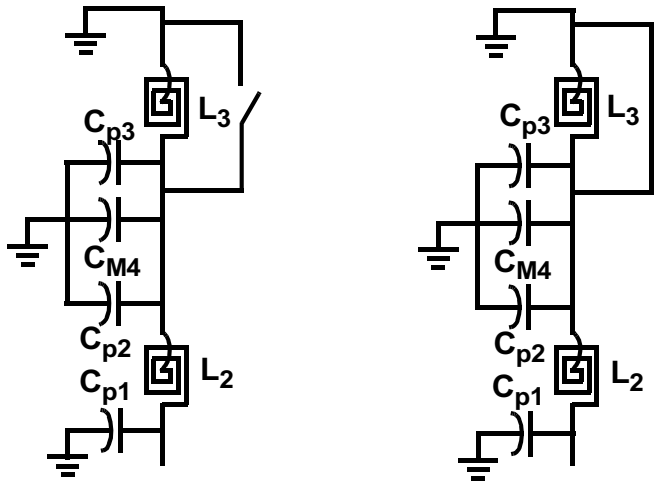


Figure 7-9 Switched resonator resonates at different bands: (a) When M4 is off, it resonates at 2.4 GHz, and (b) When M4 is on, it resonates at 5.15 GHz.

The LNA output tuning tank is a switched resonator [44], which performs band selection and gain control. The switched resonator is composed of L_2, L_3 and M_4. It resonates with the parasitic capacitance from the rest of circuit. V_{ctl} is the control voltage applied to the M_4 gate through an on-chip bias resistor R_g. Transistor M_4 acts as a switch and is toggled between the on and off states. When M_4 is turned off, the switched resonator impedance is determined by L_2 and L_3, parasitic capacitances of L_2 (C_{p1} and C_{p2}), L_3 (C_{p3}), and M_4 (C_{M4}) as illustrated in Figure 7-9(a). The parasitic capacitances from the other transistors and interconnection are not include in the figure. When M_4 is off, the total inductance is approximately the sum of L_2 and L_3. When M_4 is on, it provides a low resistance path to ac ground, therefore L_3 and C_{p2}, C_{p3} and C_{M4} are by-passed. Because of this, the effective inductance is approximately equal to L_2 as shown in Figure 7-9(b), and the capacitance looking into the structure also decreases. As discussed earlier, both inductance and capacitance are varied in a switched resonator.

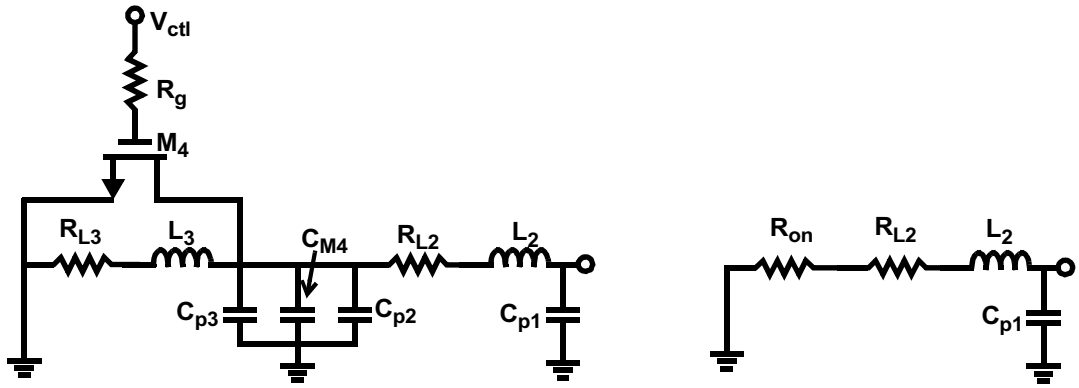
When the input signal frequency is 5.15 GHz, V_{ctl} is high and M_4 is switched on. The inductance and capacitance are low and the tank resonates near 5.15 GHz. The LNA

operates in the high gain or normal 5.15 GHz mode. If the input signal becomes strong and lower gain is needed from the LNA, then M_4 can be turned off, i.e., V_{ctl} is set low. This makes the LNA output to be tuned near 2.4 GHz, while the input is still tuned to 5.15 GHz. This causes the gain at 5.15 GHz band to be reduced. The same concept is also applicable for the 2.4 GHz band. Table 7-2 summarizes the LNA operation conditions. Each band has two gain modes: high gain mode and low gain mode. An important feature of this circuit is that the inputs stay matched in both gain modes.

The LNA input matching is similar to that used in a single band cascode LNA [78,79]. An off-chip inductor (L_{pcb1} or L_{pcb2}) in series with each input tunes out the gate-to-source capacitance (C_{gs}) at the desired band. L_1 is used to generate positive resistance, R_{in} which is approximately equal to $g_m L_1/C_{gs}$. R_{in} is approximately independent of operating frequencies which is useful for multi-band matching. Input matching network quality factor ($Q_{in}=(C_{gs}\omega_o Z_o)^{-1}$) determines power consumption, gain, noise, linearity and sensitivity to component variations [89,54]. ω_o is the operating frequency and Z_o is the characteristic impedance which is typically 50 Ω. The upper limit of Q_{in} of an LNA is usually set by the input matching consideration [55,90]. Once Q_{in} is specified, C_{gs}, thus the transistor size is specified assuming use of the minimum channel length. Unfortunately, for different applications and different frequency bands, Q_{in}'s are seldom exactly the same. Since, this dual-band LNA has two input transistors, its input matching network is

Table 7-2 LNA operation conditions

V_{ctl}	High	Low
LNA output inductance	Low	High
2.4 GHz band gain	Low	Maximum
5.15 GHz band gain	Maximum	Low



(a) (b)

Figure 7-10 M_4 (a) adds parasitic capacitance when it is off, and (b) adds series resistance with L_2 when it is on.

independently optimized for each band. The concurrent LNA [91] has only one input transistor. Its Q_{in}'s depend on operation frequencies, thus usually can not be optimize for both bands. For single band LNA's, once the common source transistor size is determined, the common-gate transistor width is set to be 60 ~ 100% of the width of the common source transistor width to minimize the noise factor [54,80,92]. For the dual band LNA, since the two parallel transistors (M_1 & M_2) increase the capacitance at the source node of the common gate transistor, this ratio is different. The size of the common gate transistor M_3 was chosen to be 84 μm in order to optimize noise figure in the both bands. This is around 50% and 100% of the widths of M_1 and M_2, respectively.

The LNA output switching resonator is also unique. The sizes of L_2, L_3 and M_4 mostly determine LNA dual-band performance, and the trade-off of sizing M_4 in the switched resonator design must be understood. Figure 7-10 shows simplified resonator circuit models when M_4 is off and on. When M_4 is off, as discussed, parasitic capacitances, C_{M4}, and C_{p2} and C_{p3} which are the parasitic capacitances of L_2 and L_3, respectively (Figure 7-10 (a)) are added to the tank. R_{L2} and R_{L3} are the parasitic series

resistances for L_2 and L_3, respectively. M_4 has channel resistance (R_{on}) which is usually on the order of a couple of ohms. When M_4 is on, this channel resistor is in series with L_2 and adds to R_{L2} as shown in Figure 7-10(b). The total quality factor (Q_{L2}) thus is degraded. Since LNA gain is approximately proportional to $L\omega Q_L$, where L is the equivalent tank inductance and Q_L is the tank quality factor, gain will decrease at given g_m when either L or Q_L decreases. To lessen this reduction in Q_L, M_4 width can be increased. However, larger M_4 increases parasitic capacitance C_{M4} when M_4 is off, which in turn decreases the effective inductance needed for a given resonant frequency. This lowers $L\omega Q_L$ or LNA gain in the low frequency band. Clearly, there are trade-offs for selecting M_4 transistor size. The size of M_4 has to be chosen to balance LNA gain in the transistor's on and off states.

In practice, the values of L_2 and L_3, and M_4 width are chosen from the LNA gain requirement. The design target for LNA gain is 23 dB in both bands. The inductance of L_2 is determined by tuning the circuit near 5.15 GHz with all the parasitic capacitance on the drain node of M_3 including the series combination of 2-pF MIM ac coupling capacitor (C_1 in Figure 7-8) and mixer RF transistor gate capacitors. Then, M_4 is chosen so that LNA voltage gain is at least 23 dB at 5.15 GHz when M_4 is on. Since M_4 is considered as a short when it is on, it does not significantly affect the resonant frequency. Lastly, L_3 is added to tune the circuit at 2.4 GHz with M_4 turned off. At the end of this process, if the gains were to have turned out to be insufficient or the imbalance between two bands is too large, g_m's of M_1 and M_2 should be re-adjusted and this process should be iterated. The final M_4 size is 315/0.18μm with R_{on} of 2.2 Ω. The control voltage for M_4, V_{ctl}, is varied between 3.6 and 1.8 V. Generation of 3.6 V requires a voltage doubler implemented with 3.3 V I/O transistors [28]. The use of 3.6 V, despite being twice the suggested supply volt-

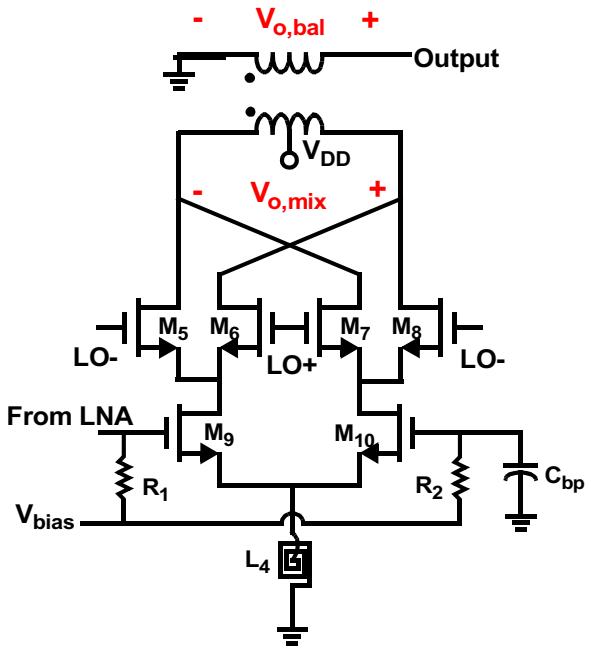


Figure 7-11 A schematic of the doubly balanced mixer.

age for the 0.18-µm CMOS process, does not result the voltage across the gate oxide to exceed 1.8 V, which ensures the long term reliability of the circuit [23,44,45].

The mixer is a doubly balanced Gilbert cell type [93] shown in Figure 7-11. M_9 and M_{10} form a differential pair with the gate of M_{10} ac grounded. C_{bp} is an on-chip bypass capacitor, and R_1, R_2 are on-chip bias resistors for RF-to-DC isolation. L_4 is an on-chip inductor to improve mixer common mode rejection. Transistors M_5-M_8 are switching transistors driven by differential LO signals. LO frequency is changed with input frequency to keep intermediate frequency (IF) fixed at 400 MHz. To drive 50 Ω measurement equipment, the mixer output signal goes directly to an off-chip center-tapped transformer/balun. In addition to differential to single end conversion, the balun transforms the 50-Ω input impedance of spectrum analyzer to 400 Ω (200 Ω for each leg). The mixer V_{DD} is connected using the secondary center tap of balun. The die photo is shown in Figure 7-12. The area is 980 x 1130 μm^2 and limited by bond pads. Compared to a

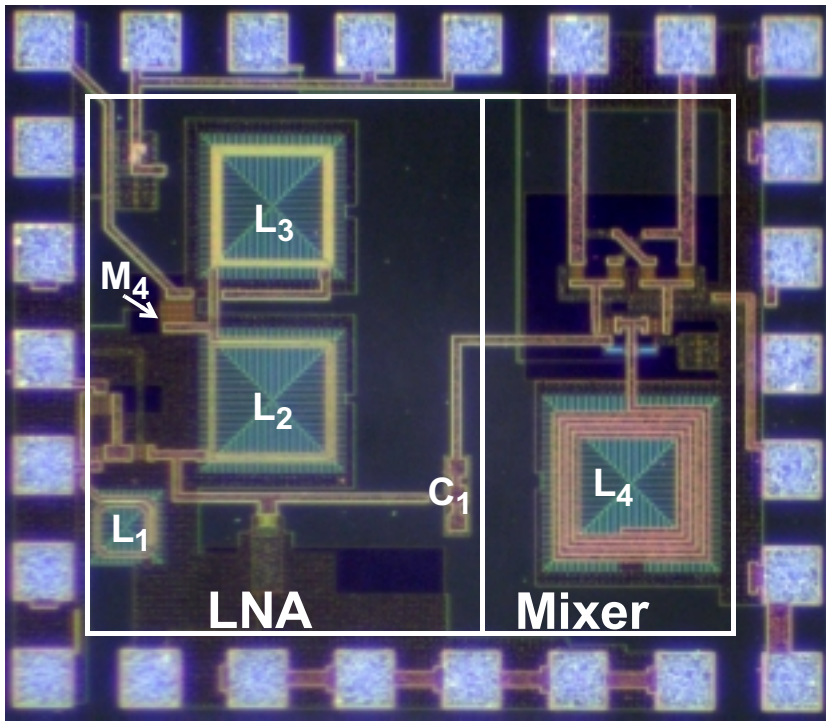


Figure 7-12 A die photograph of the dual-band RF/IF down converter. The chip area is 980x1130 μm^2 and limited by bond pads.

multi-band circuit having two sets of RF blocks, the area saving is expected to be ~ 40%, which is indeed significant.

7.3.2 Experimental Results

The RF/IF down converter circuit was tested on a four-layer FR4 board, once again using the chip-On-Board (COB) packaging technique. Figure 7-13 shows a photograph of a PCB with a die mounted on the board. The measured dual-band RF/IF down converter circuit characteristics are summarized in Table 7-3.

$|S_{11}|$'s at the 2.4 GHz and 5.15 GHz bands are given in Figure 7-14. $|S_{11}|$ is -8.0 dB at 2.4 GHz and -10.8 dB at 5.15 GHz, respectively. A 2.4 GHz band power gain versus frequency plot at the high gain mode is shown in Figure 7-15(a). The maximum conversion power gain is 26.5 dB at 2.4 GHz. When this is integrated into a receiver chain, the

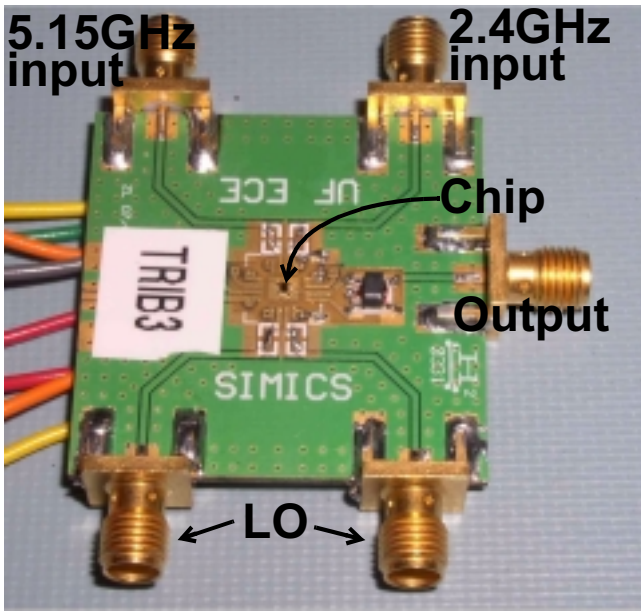


Figure 7-13 A photograph of Printed Circuit Board (PCB) with a down converter IC.

Table 7-3 Summary of the dual-band RF/IF down converter characteristics

Frequency(GHz)	2.4		5.15	
Gain Control Mode	High	Low	High	Low
Power Gain (dB)	26.5	9.5	17	10
Voltage Gain (dB)	39.8	22.8	29.2	22.2
DSB NF (dB)	1.5		4.1	
SSB NF Converted from DSB NF (dB)	2.6		6.2	
Input P_{1dB} (dBm)	-21	-17	-12	-9.5
P_{1dB} (dBm)	4.5	-8.5	4	-0.5
Input IP_3 (dBm)	-12.7	-6.6	-4.1	-1
IP_3 (dBm)	13.8	2.9	12.9	9
S_{11}(dB)	-8	-8	-10.8	-10.8
LO to IF Isolation (dB)	>30		>25	
V_{DD}(V)	1.8	1.8	1.8	1.8
LNA Current (mA)	3	3	9.1	9.1
Mixer Current (mA)	10.6	10.6	14	14

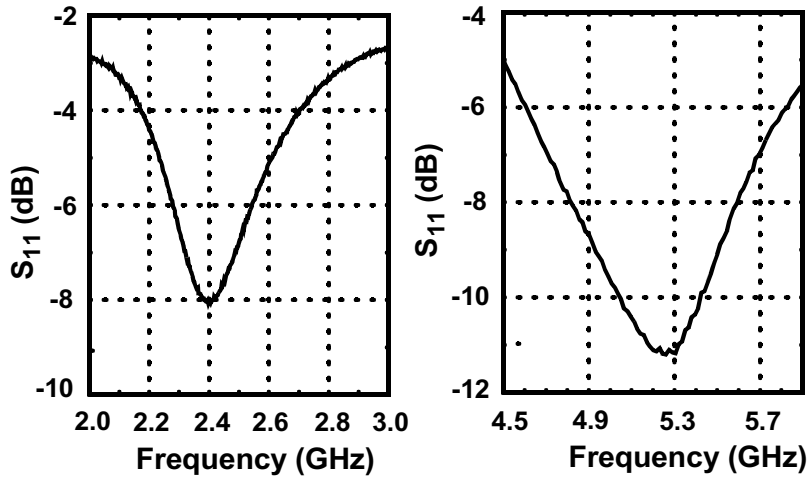


Figure 7-14 Measured input S_{11} for the dual-band RF/IF down converter. (a), S_{11}=-8 dB at 2.4 GHz (b), S_{11}=-10.8 dB at 5.15 GHz.

voltage gain ($V_{o,mix}/V_{in}$) to mixer output is more relevant. Here V_{in} is the input voltage as shown in Figure 7-8 and $V_{o,mix}$ is the differential output voltage at the mixer drain nodes shown in Figure 7-11. The corresponding voltage gain is 39.8 dB. The measured double-side band (DSB) noise figure between 2.4 and 2.48 GHz (2.4 GHz ISM band) is almost constant near 1.5 dB. Using the equation given by Winderman [94], single-side band (SSB) NF is estimated to be 2.6 dB, which is excellent. For the 2.4 GHz band operation, the LNA draws only 3 mA from a 1.8-V source.

The 5.15-GHz band measurements show that the LNA output is mis-tuned at the high gain mode. A power gain versus frequency plot is shown in Figure 7-15(b). The plot shows that the gain is peaked at a frequency lower than 5 GHz. But because of low tank Q, even with the resonant frequency lower than the design value, 17 dB power gain is still obtained at 5.15 GHz. The voltage gain is 29.2 dB and still suitable for wireless LAN applications. To increase the gain to 17 dB in the 5.15 GHz band, the bias current of the LNA was increased to 9 mA. Of course, changing bias currents for different band operation is quite permissible within the context of multi-band operation. As a matter of fact,

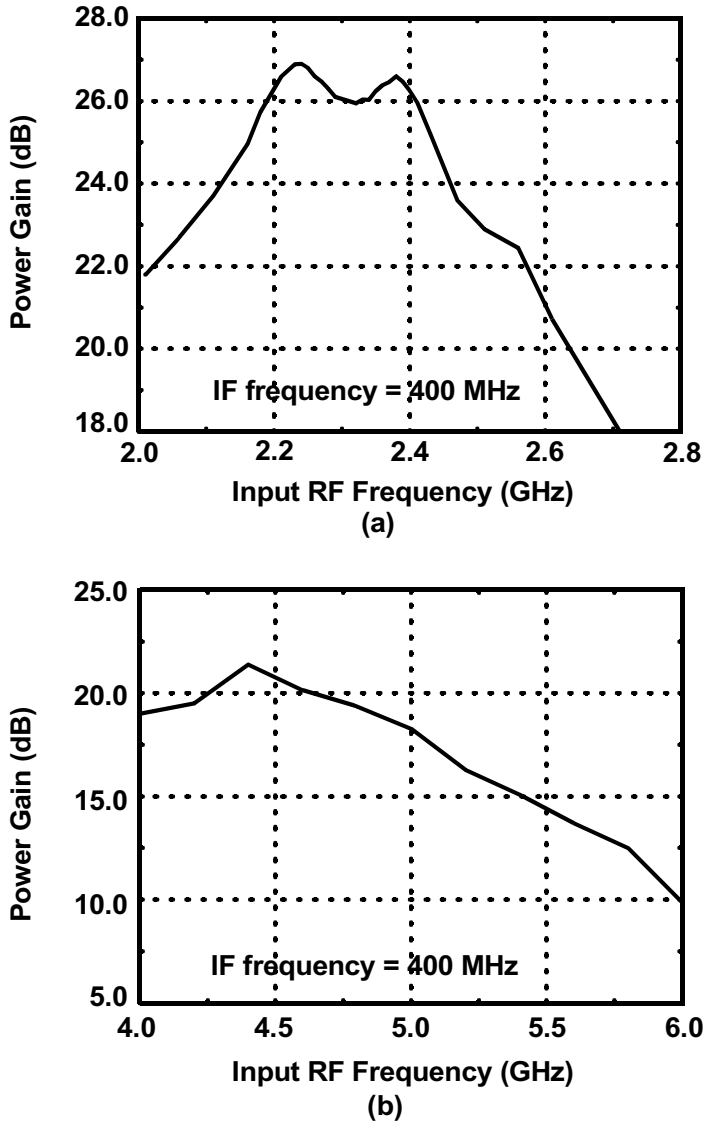
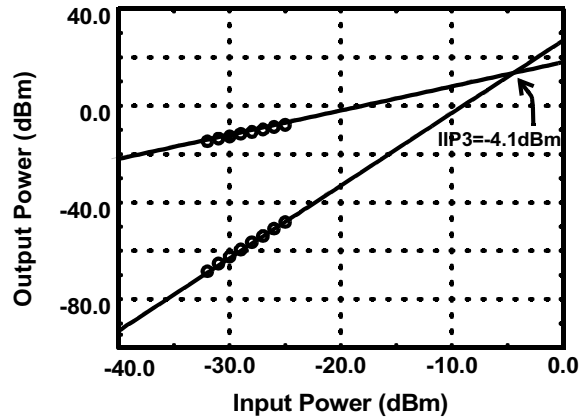
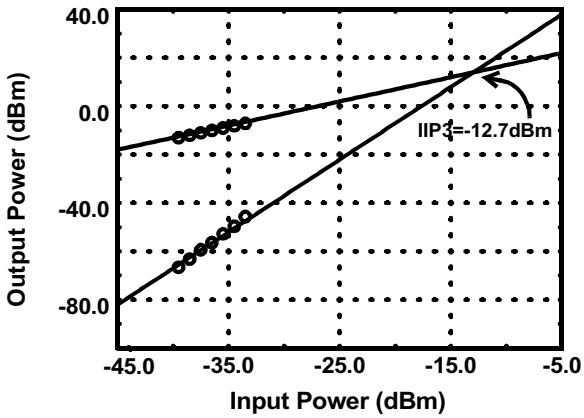


Figure 7-15 Measured power gain versus frequency for the (a) 2.4 GHz band, and (b) 5.15 GHz band.

this is desirable to lower power consumption when not necessary. This increased the gain by ~ 4 dB. Nevertheless, this circuit clearly functions as a dual-band RF front end. The measured DSB NF's between 5.15 and 5.35 GHz vary between 4.1 and 4.2 dB at the high gain mode. These when converted [94] corresponds to 6.2 to 6.3 dB SSB NF. This high noise figure is due to the gain being 8 dB lower than the design. This makes the mixer noise to play a more prominent role in determining the overall noise figure. With a 1.8-V



(a)



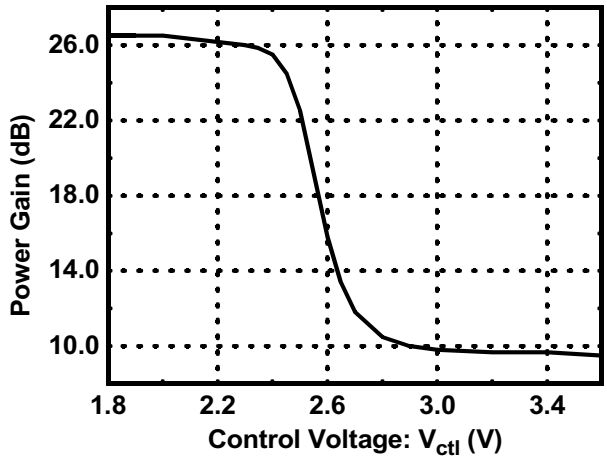
(b)

Figure 7-16 Measured input referred 3rd order intercept point (IIP3) at (a) 5.15 GHz, and (b) 2.4 GHz.

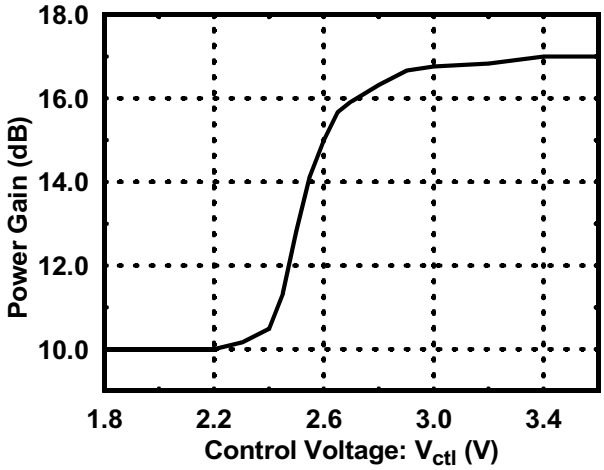
supply voltage, the circuit consumes 24 mW and 41 mW for the 2.4 GHz and 5.15 GHz band operation, respectively.

At the high gain mode, input referred P_{1dB} for 2.4 GHz and 5.15 GHz are -21 dBm and -12 dBm, respectively. Figure 7-16 shows the IIP3 plots for 5.15 GHz and 2.4 GHz operation. The input referred two-tone IP3's are -12.7 dBm and -4.1 dBm for the 2.4 and 5.15 GHz band, respectively, which are sufficient for wireless LAN applications.

The RF/IF down converter gain and linearity are also measured at the low gain mode. Figure 7-17 shows the RF/IF down converter power gain dependence on M_4 control voltage V_{ctl} at 5.15 GHz and 2.4 GHz. The power gain can be switched between 26.5



(a)



(b)

Figure 7-17 Measured RF/IF down converter power gain versus control voltage in the (a) 2.4 GHz and (b) 5.15 GHz.

and 9.5 dB for the 2.4 GHz band. The gain difference is 17 dB and could greatly help with dynamic range when the RF/IF down converter is integrated into the receiver chain. At 5.15 GHz band, the power gain in the low gain mode is 10 dB and the gain difference between that in the high and that in the low gain modes is 7 dB.

The LNA input return loss ($|S_{11}|$) are the same for all the gain control modes. This is because the cascode topology of LNA has large reverse isolation and the changes in the output matching has negligible impact on $|S_{11}|$. As discussed in section 7.2, a 5 GHz single

band LNA shows larger than 21 dB isolation. Reasonable LNA input return loss must be maintained for both the high and low gain modes since the LNA S_{11} can affect the characteristics of the preceding band pass filter (BPF).

The RF/IF down converter IIP3 improves when it operates at the low gain mode. The measured IIP3 is -6.6 dBm and -1 dBm for 2.4 GHz and 5.15 GHz, respectively. The differences from the high gain mode are ~6 and ~ 3 dB, respectively. The IIP3 is limited at the LNA input when the RF/IF down converter operates at the low gain mode. When it operates at the high gain mode, IIP3 is limited by the mixer. Because of this, the difference of IIP3 does not exactly follow the gain difference. In the low gain mode, the input referred P_{1dB} are -17 dBm and -9.5 dBm at 2.4 GHz and 5.15 GHz, respectively. It is also possible to further reduce the gain and power consumption in the low gain mode by reducing the bias currents of LNA and mixer.

7.3.3 Conclusion

A 5-GHz single band LNA fabricated in a 0.18-μm CMOS process exhibits 2.17-dB noise figure, 16.1-dB power gain with 10-mW power consumption. The input IP3 and IP2 are -4.3 dBm and 46.7 dBm, respectively. These are sufficient for wireless LAN applications. Based on this LNA, a dual-band RF/IF down converter circuit with two gain modes was designed and fabricated in a 0.18-μm CMOS process. A novel LNA with two inputs is used to handle signals in the 2.4 and 5.15 GHz bands. The band selection and gain switching are implemented by using a switching resonator. The dual-band RF/IF down converter achieves acceptable gain at both bands at the high gain operation mode. In the high gain mode, the circuit has 39.8 dB maximum voltage gain and 1.5 dB DSB NF at 2.4 GHz. In the 5.15 GHz band, the maximum voltage gain is 29.2 dB and DSB NF is 4.1

dB. At the low gain mode, voltage gain is about 22 dB for the both bands. With a 1.8-V supply voltage, the circuit consumes 24 mW and 41 mW for the 2.4 GHz and 5.15 GHz band operation, respectively. Despite the relatively high noise figure at 5.15 GHz band, the gains and noise figures are acceptable for 802.11a and 802.11b applications.

Like the multi-band CMOS VCO described in Chapter 6, this dual-band RF/IF down-converter not only demonstrates the feasibility of achieving multi-band operation in a CMOS technology, also illustrate the feasibility of using a single set of multi-band RF blocks with switched control to reduce integrated circuit area.

CHAPTER 8
A STUDY OF INJECTION LOCKING IN DIFFERENTIAL CMOS LC VCO

8.1 Introduction

Most of critical RF blocks in the proposed multi-band reciever, including RF switches, wide-tuning range VCO and divider, multi-band VCO and multi-band RF/IF down-converter, have been studied and demonstrated. The exprimental results indicate that the proposed receiver is feasible. In order to realize a fully integrated transceiver, an interested investigation of the interaction between the VCO and an external injection signal has been carried out.

When the receiver is integrated with a transmitter, a VCO and a power amplifier will be in the same die. The power amplifier usually generates a large signal. A portion of this large signal will couple into the VCO and affect the VCO. The VCO needs to provide a “pure” tone signal to the receiver and transmitter. When an external signal is injected into a VCO, VCO output can become unstable, noisy, and even be locked to this external signal. Without a clean and stable signal from a VCO, the radio fails. Sources other than the power amplifier also could perturb a VCO.

This interaction between a VCO and a external signal occurs through a mechanism called “injection locking”, also sometimes called “injection pulling” [7]. A free-running oscillator oscillates at its natural frequency in the absence of an externally applied signal. In the presence of a signal, the oscillator can synchronize with and track the input waveform. If the injected signal is close to the free-running frequency and has a comparable

magnitude then, the oscillating frequency will shift toward the injection frequency and eventually “lock” to that frequency, or “injection lock”.

Depending on the relationship between the injected frequency (ω_{inj}) and VCO oscillator frequency (ω_{lo}), the injection locking can be classified as following types:

- Fundamental injection locking $\omega_{inj} \cong \omega_{lo}$

  The injection signal is close to the oscillating frequency.

- Subharmonic injection locking $\omega_{inj} \cong \frac{1}{n} \cdot \omega_{lo}$

  The injection signal is a subharmonic of the oscillator output.

- Superharmonic injection locking $\omega_{inj} \cong n \cdot \omega_{lo}$

  The injection signal is a superharmonic of the oscillator output.

- Fractional injection locking $\omega_{inj} \cong \frac{n}{m} \cdot \omega_{lo}$

  The injection signal is a fraction of the oscillator frequency. Here *m* and *n* are integers.

The injection locking phenomena can be specified by the injection signal magnitude and locking bandwidth. The locking bandwidth is a frequency range for which an oscillator can track an injection signal. The locking bandwidth varies with the injection signal power levels. For example, if at 0dBm injection signal power, an oscillator can track the injection signal between 1.1 to 1.3 GHz, then in this case, the locking bandwidth is 200MHz. When an injection signal is increased to 5 dBm, if an oscillator can be locked between 1.05 to 1.35GHz, then the locking bandwidth is 300 MHz.

Of the many different types of oscillators, the differential LC oscillator with excellent phase noise is commonly used in RF integrated circuits, and the injection locking properties of such oscillators are of great interest. Examples of LC oscillators are the VCO’s in Chapter 5 and 6. This work presents the results of a study for injection locking

of an LC oscillator. A theoretical analysis of injection locking in a differential LC VCO is provided in section 8.2. The experimental results of VCO injection testing follow in section 8.3. The summary and conclusions are given in section 8.4. This work is intended to look for system and circuit approaches to reduce the interaction between VCO and incident signals, to provide general understanding and a set of guide for mitigating the injection locking phenomena.

8.2 Theoretical Analysis of Injecting Locking in Differential LC VCO

8.2.1 Differential LC Oscillator

An LC oscillator can be modeled as a nonlinear block *f(e)* followed by a frequency selective block (e.g., an RLC tank) with a transfer function H(ω), in a positive feedback loop as shown in Figure 8-1 [95].

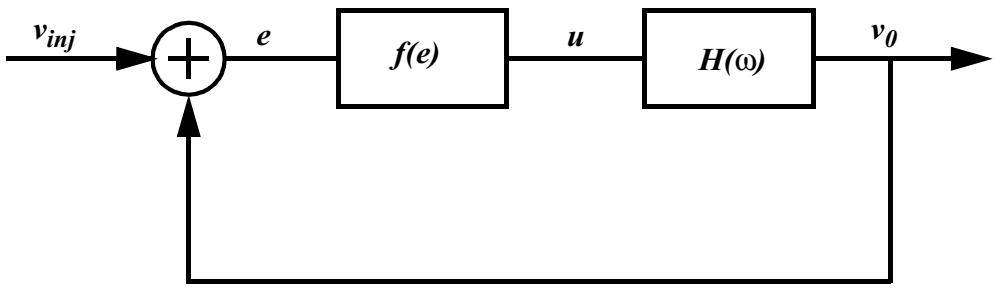


Figure 8-1 Model for an injection-locked LC oscillator

All of the non-linearities in the oscillator including any amplitude limiting mechanisms, are part of the nonlinear block, *f(e)*. To achieve steady-state oscillation, the Barkhausen criteria must be met: a loop gain of unity and a loop phase shift of 0^o or 360^o. The oscillator can not be locked if either the phase condition or the gain condition is not met.

Let us define $v_{inj}(t)=A_i\cos(\omega_{inj}t)$, $v_o(t)=A_o\cos(\omega_o t)$, $u(t)=f(e(t))=f(v_o(t)+v_{inj}(t))$, and $H(\omega)=H_o/(1+j2Q(\omega-\omega_r)/\omega_r)$, where $v_{inj}(t)$ is the injection signal, $v_o(t)$ is the output

signal, ω_r and Q are the resonant frequency and quality factor of a 2nd order RLC tank, respectively. The output of the nonlinear block *u(t)* may contain various harmonics and intermodulation terms of $v_{inj}(t)$ and $v_o(t)$. As shown by Rategh and Lee [95], the *u(t)* can be written as $u(t)=\Sigma\Sigma K_{m,n}cos(m\omega_{inj}t)cos(n\omega_o t)$, where $K_{m,n}$ is an intermodulation coefficient of $f(v_o(t)+v_{inj}(t))$.

As *u(t)* passes through a frequency selective block $H(\omega)$, **all the frequency components of *u(t)* far from the resonant frequency of tank will be filtered out.** This is generally true for LC oscillators. In this case, we only need to consider intermodulation terms generating frequency near ω_o, i.e., $|m\omega_{inj} - n\omega_o| \cong \omega_o$. In another word, **no matter what types of injection occurs, subharmonic injection or superharmonic injection, the fundamental frequency signal appearing at the tank locks the free-running oscillator** [95, 96]. This is an important assertion. Based on this, a theoretical injection locking analysis is performed for a differential LC oscillator.

The LC oscillator under study utilizes the same VCO circuit topology described in Chapter 6. Its simplified schematic is shown in Figure 8-2. Though an NMOS VCO is chosen here for analysis, the same conclusions apply for PMOS VCO's. M_1 and M_2 are the core transistors and cross coupled. M_3 is the current source. The bypass capacitor C_{bp}, which is drawn in dashed lines, is not included in the analysis. Its impact will be discussed later.

When an external signal is present, there are many points at which the signal can be injected into a VCO. As marked in Figure 8-2, A, B, C, D_1, D_2, E_1 and E_2 are critical injection points. Injection at different points will have different effects on circuit behaviors. These injection points are categorized into two groups. Points A, B, C form one

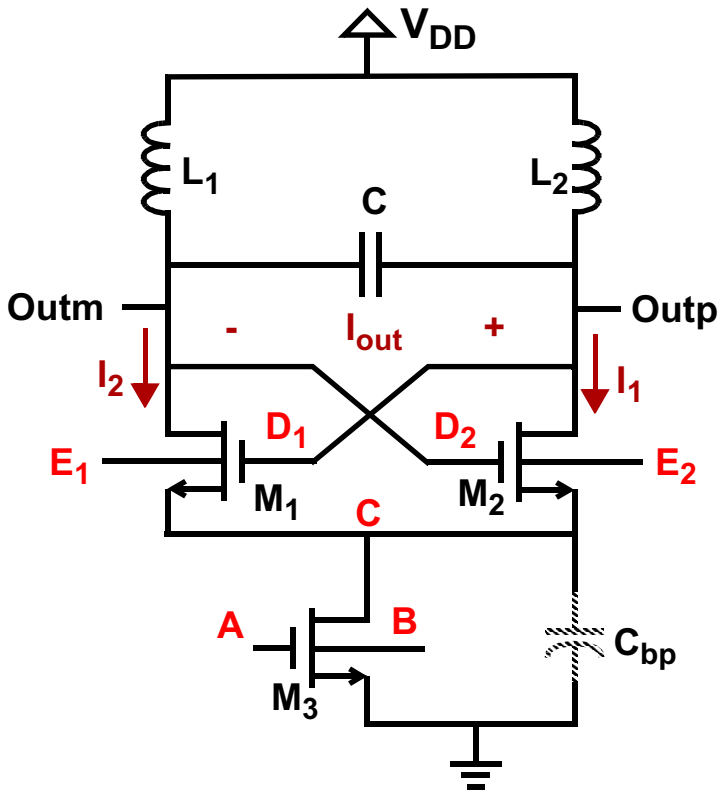


Figure 8-2 A simplified differential LC VCO schematic

group and is called "points for injection into current source", and points D_1, D_2, E_1, E_2 form another group and is called "points for injection into the core transistors."

8.2.2 Injection into the Current Source

When an injection signal appears at point A, it is easy to see that the current source acts as a common source amplifier, and amplified v_{inj} will appear at point C. For the signal injected at point B, the external signal will also be amplified or attenuated through the backgate (i.e., body) of MOS transistors, and will appear at point C. So injection from A, B and C all will cause voltage changes in point C. But an obvious question is "which node is more sensitive?" This can be easily found by redrawing the VCO as that shown in Figure 8-3.

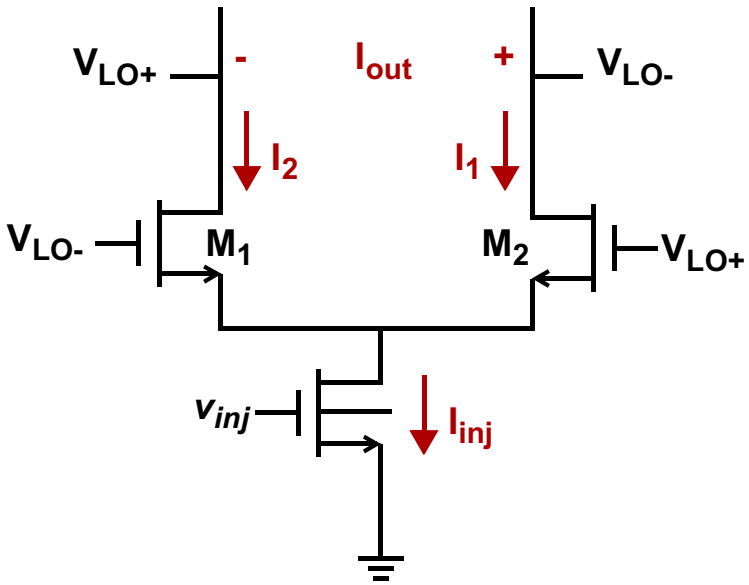


Figure 8-3 The redrawn VCO schematic

By inspection, the circuit is a single-balanced mixer. Any signal injected into the current source mixes with the LO signal or VCO output. Also depending on the injection signal frequencies, the different injection points should have different mixer gain. With the right input frequency, point A should have the largest mixer gain. Since injection into point A, B and C are essentially the same, without losing generality, point A is used to analyze how the injection into current source affects the VCO.

As illustrated in Figure 8-3, the mixer output current I_{out} can be found as

$$I_{out} = I_1 - I_2 = I_{inj} \cdot (I_1 - I_2)/(I_1 + I_2) \tag{8.1}$$

here $I_{inj}=I_1+I_2$ is the total current through the current source M_3, which is modified by the injection signal v_{inj}.

I_1 and I_2 are controlled by the gate voltages V_{LO+} and V_{LO-}, respectively. The difference of V_{LO+} and V_{LO-} is the VCO output signal, i.e.,

$$V_{LO+} - V_{LO-} = v_o = A_o \cos(\omega_o t). \tag{8.2}$$

The common mode voltage V_G of V_{LO+} and V_{LO-} can be defined as

$$V_G = 1/2 \cdot (V_{LO+} + V_{LO-}). \tag{8.3}$$

Then V_{LO+} and V_{LO-} can be expressed by V_G and v_o as

$$V_{LO+} = V_G + 1/2\ v_o \tag{8.4}$$

$$V_{LO-} = V_G - 1/2\ v_o \tag{8.5}$$

Since the voltage swing at VCO output usually is large, the MOS transistor drain current will be affected by the mobility dependence on bias, and the perfect square law drain current equation can not be used here. The modified MOS transistor drain current equation is given as [97, 55]

$$I_D = \frac{1}{2}\beta \cdot \frac{(V_{gs} - V_T)^2}{1 + \theta(V_{gs} - V_T)}, \tag{8.6}$$

where V_{gs} is $(V_{LO+} - V_S)$ for I_1 and $(V_{LO-} - V_S)$ for I_2. θ and β are technology-dependent parameters with the units of V^{-1} and A/V^2, respectively. Now we can express I_1 and I_2 as function of V_G and v_o,

$$I_1 = \frac{1}{2}\beta \cdot \frac{\left(\frac{1}{2}v_o + V_G - V_S - V_T\right)^2}{1 + \theta\left(\frac{1}{2}v_o + V_G - V_S - V_T\right)} \tag{8.7}$$

$$I_2 = \frac{1}{2}\beta \cdot \frac{\left(-\frac{1}{2}v_o + V_G - V_S - V_T\right)^2}{1 + \theta\left(-\frac{1}{2}v_o + V_G - V_S - V_T\right)}. \tag{8.8}$$

The mixer output current I_{out} can be solved by substituting Eq. (8.7) and (8.8) into Eq. (8.1), then

$$I_{out} = I_{inj} \cdot \frac{2(V_G - V_S - V_T)v_o + \theta(V_G - V_S - V_T)^2 v_o - \frac{1}{4}\theta v_o^3}{\frac{1}{2}(1 - \theta)v_o^2 + 2(V_G - V_S - V_T)^2 + 2\theta(V_G - V_S - V_T)^3} = I_{inj} \cdot f(v_o) \tag{8.9}$$

where the second term is defined as $f(v_o)$. $f(v_o)$ is a non-linear function of v_o and can be expanded by using the Taylor series. Thus $f(v_o)$ can also be expressed as

$$f(v_o) = b_0 + b_1 v_o + b_2 v_o^2 + b_3 v_o^3 + b_4 v_o^4 + b_5 v_o^5 + ... \quad (8.10)$$

where b_0, b_1, b_2, b_3... are coefficients of this polynomial.

I_{inj} is the function of the injected signal v_{inj} and can be expressed with as a power series,

$$I_{inj} = a_0 + a_1 v_{inj} + a_2 v_{inj}^2 + a_3 v_{inj}^3 + a_4 v_{inj}^4 + ... \quad (8.11)$$

So it is clear the mixer output is composed of the products of an injection signal v_{inj} and an VCO oscillating signal v_o. The mixer output current I_{out} is

$$\begin{aligned} I_{out} &= I_{inj} \cdot f(v_o) \\ &= (a_0 + a_1 v_{inj} + a_2 v_{inj}^2 + a_3 v_{inj}^3 + a_4 v_{inj}^4 + ...) \cdot \\ &\quad (b_0 + b_1 v_o + b_2 v_o^2 + b_3 v_o^3 + b_4 v_o^4 + b_5 v_o^5 + ...) \end{aligned}$$

In reality, the high order harmonics are smaller. The analysis can be simplified without greatly sacrificing accuracy by considering up to 4th order harmonics. In this case,

$$I_{out} = (a_0 + a_1 v_{inj} + a_2 v_{inj}^2 + a_3 v_{inj}^3 + a_4 v_{inj}^4) \cdot (b_0 + b_1 v_o + b_2 v_o^2 + b_3 v_o^3 + b_4 v_o^4) \quad (8.12)$$

As defined earlier,

$$v_{inj} = A_i \cos(\omega_{inj} t) = A_i \cos\alpha \quad (8.13)$$

$$v_o = A_o \cos(\omega_o t) = A_o \cos\beta \quad (8.14)$$

Here, A_i is the amplitude of injection signal and A_o is the amplitude of oscillating signal, ω_{inj} and ω_o are the injection and oscillating frequencies, respectively.

Now by substituting v_{inj}, v_o into Eq. (8.12), I_{out} is

$$I_{out} = \ldots + \cos\alpha\,(a_1A_i+3/4a_3A_i^3)(b_0+1/2b_2A_o^2+3/8b_4A_o^4) +$$
$$\cos\alpha\cos\beta\,(a_1A_i+3/4a_3A_i^3)(b_1A_o+3/4b_3A_o^3) +$$
$$\cos2\alpha\,(1/2a_2A_i^2+1/2a_4A_i^4)(b_0+1/2b_2A_o^2+3/8b_4A_o^4) +$$
$$\cos2\alpha\cos\beta\,(1/2a_2A_i^2+1/2a_4A_i^4)\,(b_1A_o+3/4b_3A_o^3) +$$
$$\cos3\alpha\cos\beta\,(1/4a_3A_i^3)\,(b_1A_o+3/4b_3A_o^3) +$$
$$\cos4\alpha\cos\beta\,(1/8a_4A_i^4)\,(b_1A_o+3/4b_3A_o^3) + \ldots \qquad (8.15)$$

As mentioned earlier, the terms near the fundamental frequency in I_{out} will be selected by the LC tank and other terms will be filtered out. So the selected terms have to satisfy the equation $|m\omega_{inj} - n\omega_o| = (\omega_o \pm \Delta\omega) \cong \omega_o$. Depending on the injection signal frequencies, any terms in Eq. (8.15), such as $\cos2\alpha\cos\beta$, $\cos3\alpha\cos\beta$ could generate a signal tone $\omega_o \pm \Delta\omega$ near the oscillating frequency (ω_o). But comparing to ω_o, the $\Delta\omega$ is much smaller, usually less than 1% of ω_o. Thus all coefficients in Eq. (8.12), such as a_0, a_1, a_2, a_3, a_4, b_0, b_1, b_2, b_3 and b_4 at $\omega_o \pm \Delta\omega$ are the same as those at ω_o. Thus, the condition for locking can be calculated at the point $|m\omega_{inj}-n\omega_o|=\omega_o$. This is also true if the free-running VCO has already been locked. Under this condition, let us look at the terms which generate the fundamental tone for the different injection types.

8.2.2.1 Subharmonic injection locking

The 2nd subharmonic, i.e., $\omega_{inj} \cong 1/2 \cdot \omega_o$, is used as an example for the subharmonic injection analysis. The condition for locking is

$$|m\omega_{inj} - n\omega_o| \cong |1/2 \cdot m\omega_o - n\omega_o| = \omega_o, \qquad (8.16)$$

and then $|1/2 \cdot m - n| = 1$. The smallest m and n to satisfy this condition are 2 and 0, respectively. The m=2 and n=0 corresponds to the $\cos2\alpha$ term. The coefficient of $\cos2\alpha$ term is $(1/2a_2A_i^2+1/2a_4A_i^4)(b_0+1/2b_2A_o^2+3/8b_4A_o^4)$. From Eq. (8.10), if $f(v_o)$ is a square

wave with 50% cycle duty, coefficients b_0, b_2 and b_4 should be zero. In reality, with differential VCO topology, the even order coefficients b_0, b_2 and b_4 will be smaller than the odd order coefficients b_1 and b_3. So another set of m and n has to be considered to give the dominant term for the mixer gain of 2nd subharmonic injection locking. This set is m=4 and n=1, which corresponds to the $\cos4\alpha\cos\beta$ term. The coefficient of $\cos4\alpha\cos\beta$ term is $1/2\cdot(1/8a_4A_i^4)\ (b_1A_o+3/4b_3A_o^3) = K_{core}(1/8a_4A_i^4)$, where $K_{core}=1/2\cdot(b_1A_o+3/4b_3A_o^3)$. We ignore the other sets of m, n which satisfy the Eq. (8.16) because they represent even higher order products and have much small gain. The coefficients of $\cos2\alpha$ and $\cos4\alpha\cos\beta$ terms are the mixer gain for 2nd subharmonic injection locking, so

$$K_{sub} = 1/2\cdot(1/8a_4A_i^4)\ (b_1A_o+3/4b_3A_o^3) + (1/2a_2A_i^2 +1/2a_4A_i^4)(b_0+1/2b_2A_o^2+3/8b_4A_o^4)$$

In most case $a_2 >> a_4$, and $b_0 >> b_2 >> b_4$, thus

$$K_{sub}=\sim K_{core}(1/8a_4A_i^4) + 1/4a_2b_2A_i^2A_o^2$$

8.2.2.2 Fundamental injection locking

The fundamental injection locking occurs when $\omega_{inj} \cong \omega_o$. The condition for locking is $| m\omega_{inj}-\omega_o | = \omega_o$. So,

$$\left|m\omega_{inj} - n\omega_o\right| \cong \left|m\omega_o - n\omega_o\right| = \omega_o, \tag{8.17}$$

and then $| m - n | = 1$. The smallest m and n to satisfy this condition are 1 and 0, respectively. This corresponds to the $\cos\alpha$ term in the mixer output. The coefficient of $\cos\alpha$ is $(a_1A_i+3/4a_3A_i^3)(b_0+1/2b_2A_o^2+3/8b_4A_o^4) \sim b_o(a_1A_i+3/4a_3A_i^3)$ because usually $b_0>>b_2>>b_4$. The $\cos\alpha$ term corresponds to RF-to-IF feedthrough in a mixer circuit. The generation of $\cos\alpha$ is determined by the symmetry of circuit. It depends on transistor mismatch, operating points, the symmetry of oscillating signal, etc. In reality, even for a dou-

ble-balanced Gilbert-cell mixer, the RF-IF isolation can be as bad as only 8 dB [98]. Thus, this term can not be simply ignored and must be included.

The next set of m and n to satisfy the equation is m=2 and n=1. This corresponds to the cos2αcosβ term in the mixer output. The coefficient of cos2αcosβ is

$$1/2\cdot(1/2a_2A_i^2+1/2a_4A_i^4)\,(b_1A_o+3/4b_3A_o^3)$$

Once again the higher number of m and n are ignored assuming the small contribution. Thus the mixer gain for the fundamental injection locking is

$$K_{fund} = 1/2\cdot(1/2a_2A_i^2 +1/2a_4A_i^4)\,(b_1A_o+3/4b_3A_o^3)+b_o(a_1A_i+3/4a_3A_i^3)$$

In most case $a_1 >> a_2 >> a_3 >> a_4$, thus

$$K_{fund} =\sim K_{core}\,(1/2a_2A_i^2) + a_1b_oA_i.$$

8.2.2.3 Superharmonic injection locking

For example, if $\omega_{inj} \cong 2\omega_o$, The condition for locking is

$$\left|m\omega_{inj} - n\omega_o\right| \cong \left|2m\omega_o - n\omega_o\right| = \omega_o, \tag{8.18}$$

and then $|2m - n| = 1$. The smallest m and n to satisfy this condition are 1 and 1, respectively. This corresponds to the cosαcosβ term in mixer output. So the coefficient of cosα cosβ is the mixer gain for 2nd superharmonic injection locking, and

$$K_{super} = 1/2\cdot(a_1A_i+3/4a_3A_i^3)(b_1A_o+3/4b_3A_o^3)$$

$$=\sim K_{core}\,(a_1A_i) \qquad \text{since a1 >> a3}$$

8.2.2.4 Fractional injection locking (case 1)

We will treat two fractional injection locking cases. First look at $\omega_{inj} \cong 2/3 \cdot \omega_o$ case. The condition for locking is

$$\left|m\omega_{inj} - n\omega_o\right| \cong \left|\frac{2}{3}m\omega_o - n\omega_o\right| = \omega_o, \tag{8.19}$$

Table 8-1 A summary for the injection into the VCO current source.

Index	Injection Type	Product term	Gain
A	Subharmonic injection $\omega_{inj} = 1/2\ \omega_o$	$\cos4\alpha\cos\beta$ and $\cos2\alpha$	$K_{core}(1/8a_4A_i^4) + 1/4a_2b_2A_i^2A_o^2$
B	fundamental injection $\omega_{inj} = \omega_o$	$\cos2\alpha\cos\beta$ and $\cos\alpha$	$K_{core}(1/2a_2A_i^2)+a_1b_oA_i$
C	superharmonic injection $\omega_{inj} = 2\ \omega_o$	$\cos\alpha\cos\beta$	$K_{core}(a_1A_i)$
D	fractional injection $\omega_{inj} = 2/3\ \omega_o$	$\cos3\alpha\cos\beta$	$K_{core}(1/4a_3A_i^3)$
E	fractional injection $\omega_{inj} = 3/2\ \omega_o$	$\cos2\alpha\cos2\beta$	$1/8a_2b_2A_i^2A_o^2$

Note: $K_{core} = 1/2\cdot(b_1A_o+3/4b_3A_o^3)$

and then $|2/3 \cdot m - n| = 1$. The smallest m and n to satisfy this condition are 3 and 1, respectively. This corresponds to the $\cos3\alpha\cos\beta$ term in mixer output. So the coefficient of $\cos3\alpha\cos\beta$ term is the mixer gain for 2/3 fractional injection locking

$$K_{2/3} = 1/2\cdot(1/4a_3A_i^3)\ (b_1A_o+3/4b_3A_o^3) = K_{core}(1/4a_3A_i^3)$$

8.2.2.5 Fractional injection locking (case 2)

Secondly, let us look at $\omega_{inj} \cong 3/2 \cdot \omega_o$ case. The condition for locking is

$$|m\omega_{inj} - n\omega_o| \cong \left|\frac{3}{2}m\omega_o - n\omega_o\right| = \omega_o, \tag{8.20}$$

and then $\omega_{inj} \cong 3/2 \cdot \omega_o$. The smallest m and n to satisfy this condition are 2 and 2, respectively. This corresponds to the $\cos2\alpha\cos2\beta$ term in mixer output. The coefficient of $\cos2\alpha\cos2\beta$ term is $1/2\cdot(1/2a_2A_i^2 + 1/2a_4A_i^4)\cdot(1/2b_2A_o^2 +1/2b_4A_o^4)$. By ignoring higher order coefficients,

$$K_{3/2}=\sim 1/2\cdot(1/2a_2A_i^2)\ (1/2b_2A_o^2)=1/8a_2b_2A_i^2A_o^2$$

The summary of all mixer gains for different types of injection locking is given in

Table 8-1. From the above analyses, several observations can be made for a signal injected into the current source:

1) If $f(v_o)$ is a square wave with 50% cycle duty, i.e., $b_0,b_2,b_4... = 0$, A, B, C, D can be easily compared since they only differ by the current source gain coefficient a_1, a_2, a_3, a_4 and the injection signal amplitude A_i. Usually $a_1A_i > a_2A_i^2 > a_3A_i^3 > a_4A_i^4$, it is expected that the impact of 2nd subharmonic injection is the weakest, and that of the 2nd superharmonic injection is the strongest (i.e., the largest locking bandwidth). The impact of scenario D is expected to be in between those two.
2) The fundamental injection should have smaller locking bandwidth than the 2nd super-harmonic if $b_0=0$. But in reality, asymmetries of circuits will generate the fundamental signal at the output, which will increase the fundamental injection locking bandwidth.
3) The impact of scenario A and E also depend on the even order coefficient of $f(v_o)$. But the gain is determined by $a_2b_2A_i^2A_o^2$, they should have smaller locking bandwidth than fundamental injection whose gain is partially dependent on a_1b_o.
4) A possible way to eliminate all gains ($a_1=a_2=a_3=a_4=... =0$) is to place a bypass capacitor at the drain node of current source. As shown in Figure 8-2 with dashed lines, with C_{bp}, the mixer gain should be zero for any harmonics.
5) It is known that the noise from current source will corrupt VCO phase noise. However, only noise around even order harmonics of oscillating frequency, like $2\omega_o$, $4\omega_o$, $6\omega_o$..., have significant effects. The bypass C_{bp} attenuates the high-frequency noise components from the current source, so the corresponding attenuation of phase noise is also expected.

6) Though the whole derivation is based on the injected signal at the gate of current source, the similar results will be obtained when a pulling signal is injected into the current source substrate (Point B) and drain (Point C), but coefficients such as a_0, a_1, a_2, a_4... will be different for different injection points.
7) Five injection locking cases have been discussed in this subsection. More general results can be easily obtained based on the theoretical analyses. For example, if the 3rd order superharmonic is injected, in order to lock to it, the equation $| m\omega_{inj} - n\omega_o | = \omega_o$ has to be once again satisfied. So $| 3\, m\cdot\omega_o - n\cdot\omega_o | = \omega_o$, and the smallest integers for m and n are 1 and 2, respectively. This corresponds to the $\cos\alpha\cos2\beta$ term. It is not difficult to derive that the coefficient is $1/2(a_1A_i+3/4a_3A_i^3)(1/2b_2A_o^2 +1/2b_4A_o^4)$. If we still assuming the higher order coefficients is smaller than the lower order coefficient, we should expect the mixer gain of this to be larger than that of scenario E but smaller than that of 2nd superharmonic injection.
8) For the 2nd order superharmonic injection, it is shown in Rategh and Lee [95], that the locking range is proportion to the tank output impedance/Q. That means, to improve the immunity to locking, smaller inductor with the highest Q should be utilized.

8.2.3 Injection into the Core Transistors

When signals are injected into the core transistors, it can be into gates, drains or substrates. Since gates and drains are cross coupled, they are the same injection points. For the sake of simplicity, the injection into gates is used as an example to illustrate locking due to injection into core transistors. The VCO schematic is redrawn in Figure 8-4.

In the schematic, v_{op} and v_{om} are differential oscillating signals. v_{ip} and v_{im} are injected signals, which can be differential or common mode. The VCO output is

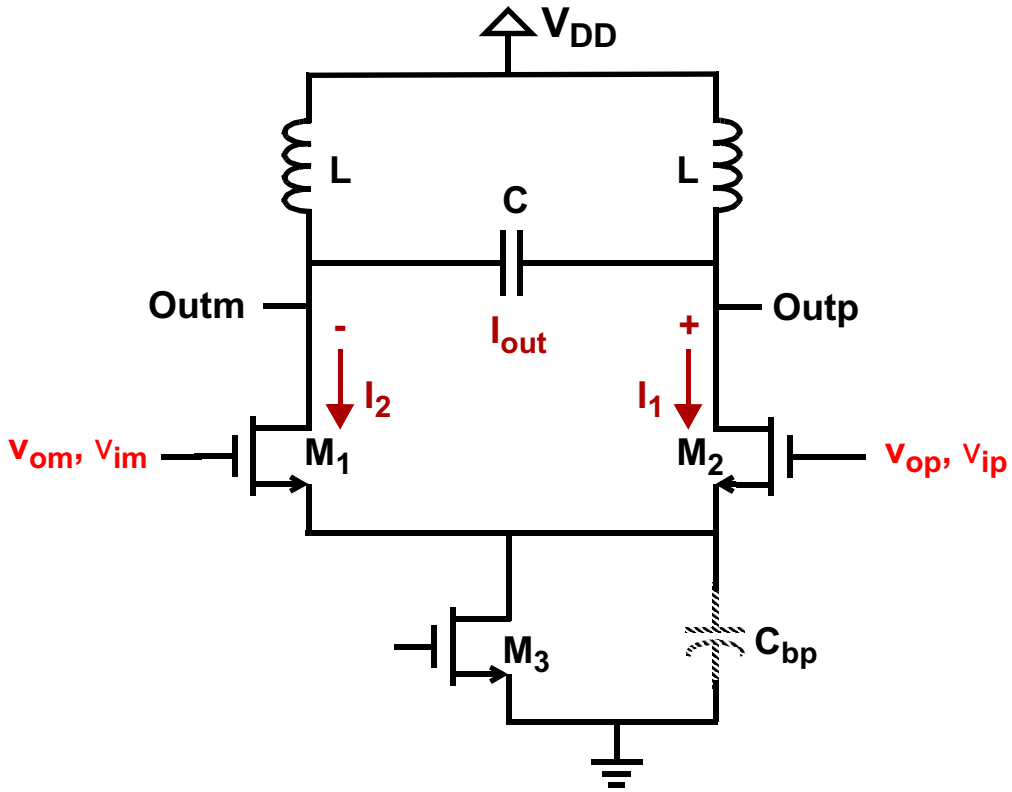


Figure 8-4 Redrawn VCO schematic to show the injection into core transistor

$I_{out} = I_1 - I_2$

$= a_{0,M1} + a_{1,M1}(v_{om}+v_{im}) + a_{2,M1}(v_{om}+v_{im})^2 + a_{3,M1}(v_{om}+v_{im})^3 + a_{4,M1}(v_{om}+v_{im})^4 + a_{5,M1}(v_{om}+v_{im})^5$

$- a_{0,M2} - a_{1,M2}(v_{op}+v_{ip}) - a_{2,M2}(v_{op}+v_{ip})^2 - a_{3,M2}(v_{op}+v_{ip})^3 - a_{4,M2}(v_{op}+v_{ip})^4 - a_{5,M2}(v_{op}+v_{ip})^5$

Here, $a_{n,M1}$ and $a_{n,M2}$ are the coefficients of nth order terms for M_1 and M_2, respectively; and n is an integer. Once again, the harmonics higher than the 4th order will be ignored. But later we will see that the 2nd subharmonic injection depends on the 5th order coefficient a_5, so 5th order harmonic terms are included in the I_{out} here for a better comparison. If the circuits are perfectly symmetric, then $a_{n,M1} = a_{n,M2} = a_n$. For the injection into the core transistors, the injected signals at the gates of transistors, v_{ip} and v_{im}, can always be expressed by a combination of a common mode signal and a differential mode signal. The

Table 8-2 A summary of the common mode injection into the core transistors

Index	Injection Type	Product term	Gain
A	Subharmonic injection $\omega_{inj} = 1/2\ \omega_o$	$\cos4\alpha\cos\beta$	$5/8a_5A_0A_i^4$
B	fundamental injection $\omega_{inj} = \omega_o$	$\cos2\alpha\cos\beta$ and $\cos\alpha$	$3/2a_3A_0A_i^2 + 5/2a_5A_0A_i^4 + 15/4a_5A_0^3A_i^2 + \Delta a_1A_i$*
C	superharmonic injection $\omega_{inj} = 2\ \omega_o$	$\cos\alpha\cos\beta$	$2a_2A_0A_i + 3a_4A_0A_i^3 + 3a_4A_0^3A_i$
D	fractional injection $\omega_{inj} = 2/3\ \omega_o$	$\cos3\alpha\cos\beta$	$a_4A_0A_i^3$
E	fractional injection $\omega_{inj} = 3/2\ \omega_o$	$\cos2\alpha\cos2\beta$	Depends on match between $a_{n,M1}$ and $a_{n,M2}$

* $\Delta a_1 = |a_{1,M1} - a_{1,M2}|$, is the mismatch of a_1 between M_1 and M_2.

circuit behaviors are different for the common mode injection and differential mode injection, and are treated separately below.

8.2.3.1 Common mode injection into core transistors

For the common mode injection, $v_{ip} = v_{im}$ and $v_{op} = - v_{om}$. For convenience, v_{op}-v_{om} is defined as v_o and $v_{ip} = v_{im}$ as v_i. Under this condition, I_{out} can be expressed as

$$I_{out}=a_1v_o+a_2(2v_ov_i)+a_3(v_o^3+3v_ov_i^2)+a_4(4v_o^3v_i+4v_ovi^3)+a_5(v_o^5+10v_o^3v_i^2+5v_ov_i^4)$$

Again, let $v_i = A_i\cos\alpha$, and $v_o = A_o\cos\beta$. Once the coefficients of $\cos m\alpha\cos n\beta$ products are derived, the relative importance of different types of locking can be evaluated. The results for the common-mode injection into core transistor are listed in Table 8-2.

8.2.3.2 Differential mode injection into core transistors

For the differential mode, $v_{ip} = - v_{im}$. Defining $v_{op} - v_{om} = v_o$ and $v_{ip} - v_{im} = v_i$,

$$I_{out} = a_1v_o + a_1v_i + a_3v_o^3 + 3a_3v_o^2v_i + 3a_3v_ov_i^2 + a_3v_i^3,$$

Table 8-3 Summery of the differential mode injection into the core transistors

Index	Injection Type	Product term	Gain
A	Subharmonic injection $\omega_{inj} = 1/2\ \omega_o$	$\cos4\alpha\cos\beta$	$5/8a_5A_0A_i^4$
B	fundamental injection $\omega_{inj} = \omega_o$	$\cos2\alpha\cos\beta$ and $\cos\alpha$	$a_1A_i+3/2a_3A_0A_i^2 + 5/2a_5A_0A_i^4+5a_5A_0^3A_i^2$
C	superharmonic injection $\omega_{inj} = 2\ \omega_o$	$\cos\alpha\cos\beta$	Depends on match between $a_{n,M1}$ and $a_{n,M2}$
D	fractional injection $\omega_{inj} = 2/3\ \omega_o$	$\cos3\alpha\cos\beta$	Depends on match between $a_{n,M1}$ and $a_{n,M2}$
E	fractional injection $\omega_{inj} = 3/2\ \omega_o$	$\cos2\alpha\cos2\beta$	Depends on match between $a_{n,M1}$ and $a_{n,M2}$

Once again, substituting $v_i = A_i\cos\alpha$ and $v_o = A_o\cos\beta$, and all the coefficients for the different types of injections are derived. The summary is given in Table 8-3.

From Table 8-2 and Table 8-3, several observations can be made for the injection into the core transistors:

1) For the common mode injection into the core transistors, assuming the lower order gain is higher, e.g. $a_2 > a_3 > a_4 > a_5$, one expects the weakest injection is the 2nd order subharmonic injection and the worst is the 2nd order superharmonic injection. The robustness against injection improves in the following order if the circuit is symmetric: fundamental injection, 2/3 fractional injection and 2nd order subharmonic injection. The 3/2 fractional injection and the fundamental injection depend on circuit symmetry.
2) For the differential mode injection into core transistors, VCO is most susceptible to the fundamental injection. The 2nd order superharmonic and 2/3 and 3/2 fractional injections depend on the circuit symmetry. The 1/2 subharmonic injection depends on the 5th order products and is expected to be small.

3) The signals injected into the core transistors can not be bypassed. In order to reduce the signal coupling, various isolation techniques may be used to protect the VCO core: shielded VCO tank, a heavy guard ring around VCO core transistors, PMOS (n-well) or NMOS (deep-n-well) devices in isolated wells.

Injection locking is a fundamental property of a VCO. For different types of injection, the circuit will have varying responses. A theoretical framework for analyzing LC oscillator injection locking is proposed. In many situations, the responses depend on the circuit symmetry. The injection signal magnitude also depends on the impedance between the injection point and circuit. These depend on actual implementation. Because of this, a real VCO circuit which can be tested for the injection locking should be included in the study. The experimental study could test the theoretical analyses. The testing circuits always provide more insights. In addition, new techniques to reduce the VCO injection locking can be discovered through the testing circuits. This could provide the guideline for future circuit design. Thus, based on the theoretical analyses, a set of VCO injection locking testing circuits is implemented, and their characteristics are discussed in the next section.

8.3 Testing of Injection Locking in Differential LC VCO

8.3.1 The Injection Locking Test Circuits

The VCO's for injection locking test have been fabricated in a 0.18-μm CMOS technology. All VCO's have the same schematic, which is illustrated in Figure 8-5. The VCO's utilize an all NMOS differential LC VCO topology. The VCO core is the same as the simplified VCO schematic shown in Figure 8-2 used for the theoretical analyses, except the added bias circuitry for the VCO core. M_3 and M_4 form a current mirror. To

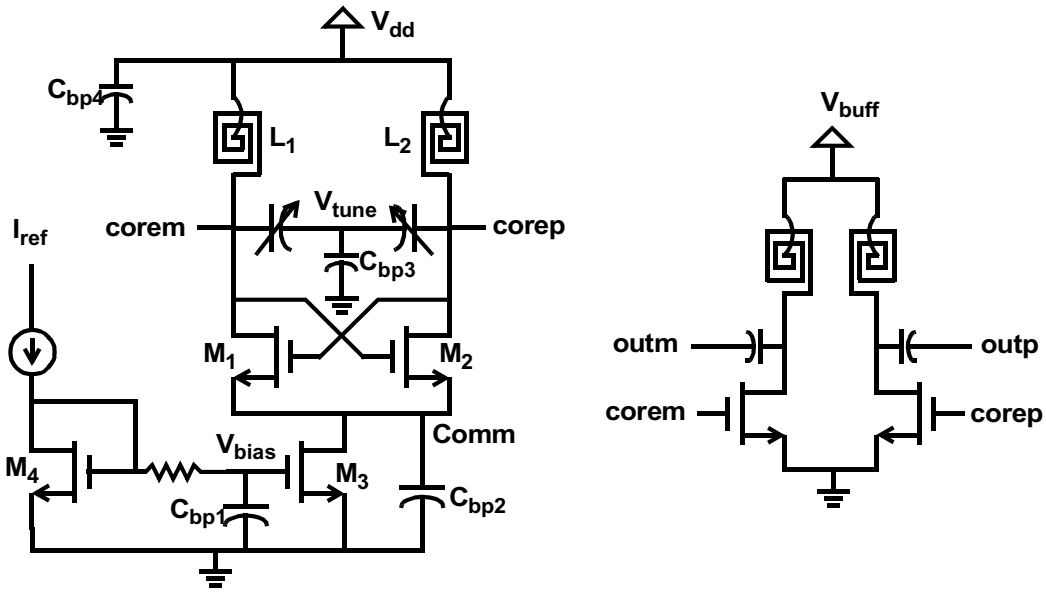


Figure 8-5 The schematic of the injection locking testing VCO. It shows (a) VCO core with the bias circuitry, and (b) VCO output buffer.

drive the measurement equipment, a common-source differential buffer is integrated with the VCO as shown in Figure 8-5(b). Several on-chip bypass capacitors are placed around VCO circuit: one is on V_{bias} node (C_{bp1}), one on "comm" node (C_{bp2}), one on V_{tune} node (C_{bp3}) and one on V_{DD} node (V_{bp4}). These bypass capacitors are intentionally designed such that they can be cut by a laser after the fabrication.

The VCO inductors L_1 and L_2 were built by using a differential inductor [64]. The differential inductor is smaller and could reduce the magnetic coupling through the silicon substrate. Two types of differential inductors are used in VCO's. The first type of the differential inductor is a regular planar on-chip inductor with metal 4 and metal 5 layers shunted together. The second type include a ground shield around the first type inductor. The ground shield is made by poly and metal 6 layers with vias connecting them. The second inductor type is called a "fully-ground-shielded" inductor and is illustrated in Figure 8-6. Both the poly and metal 6 are patterned ground shields [51] to reduce the eddy

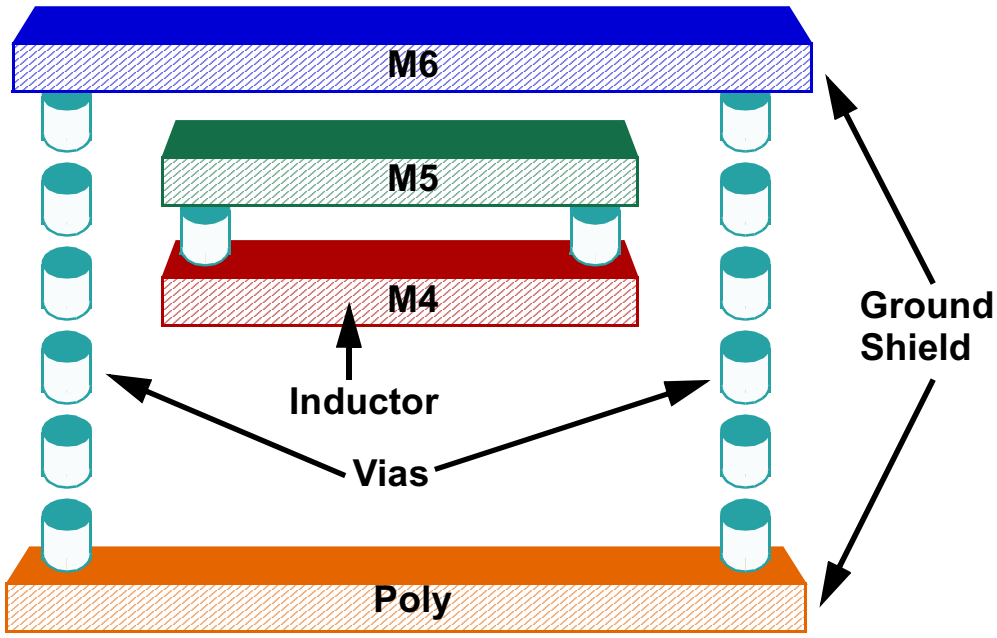


Figure 8-6 A fully-ground-shielded inductor: the inductor is inside a ground shield composed of poly, vias and metal 6

current. The purpose of adding a ground shield is to evaluate shielding techniques for on-chip VCO since the shielding is commonly used in discrete VCO design.

Another technique frequently used to improve chip isolation is the use of p^+ guard rings, i.e., a large number of substrate contacts, surrounding the NMOS transistors. To evaluate this effect, a VCO with a large p^+ guard ring and another one with minimal substrate contacts required by the design rule have been implemented.

Total three VCO's have been implemented. The first VCO has a fully-ground-shielded differential inductor and its transistors surrounded with large guard rings. This VCO is the one with the standard layout and called VCO_standard. The difference between the first and the second VCO is that the second VCO uses the regular differential inductor without any ground shield. This VCO is named VCO_ind for short. The third VCO did not use a guard ring around the transistors while keeping the rest of layout

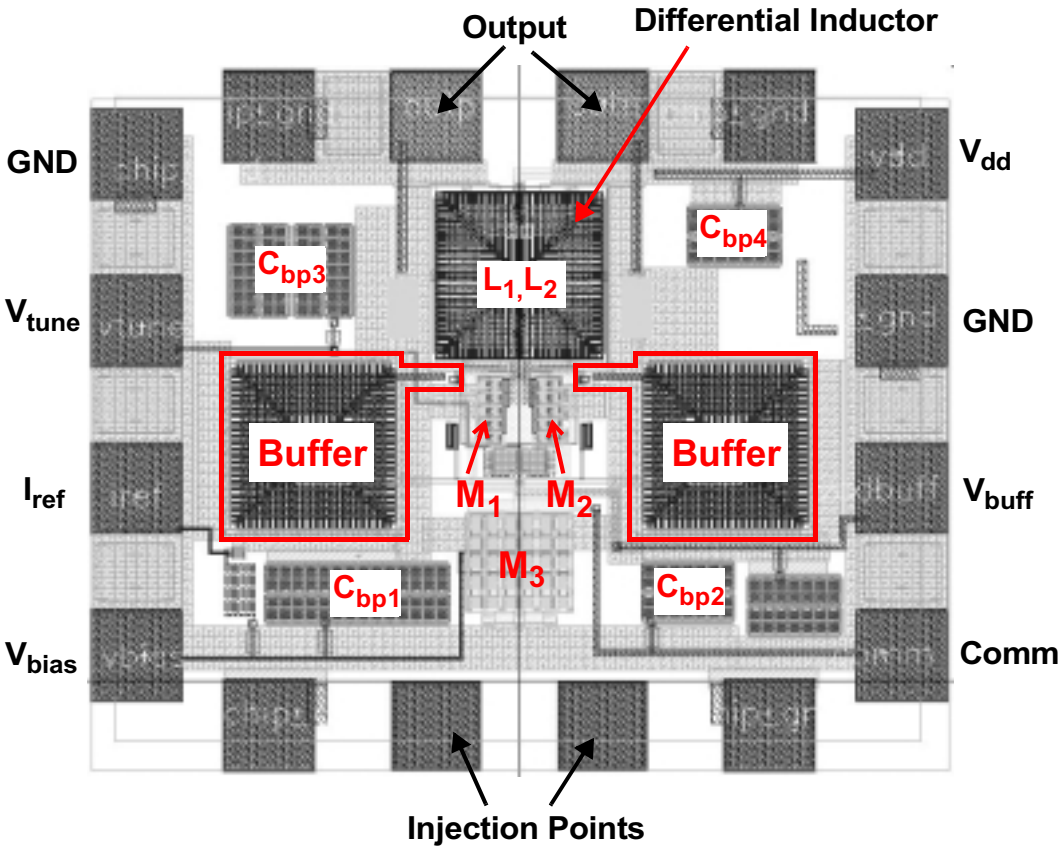


Figure 8-7 The layout of VCO_standard. It uses a differential GSSG pad frame as the injection points.

the same as VCO_standard. This VCO is called VCO_subcont to indicate that it has the minimal substrate contacts.

8.3.2 Injection Locking Testing Setup

In order to perform the injection locking testing an external injection point is placed near by the VCO. The layout of VCO_standard is shown in Figure 8-7 to illustrate this. A GSSG differential pad is used for injection, which is symmetric along the VCO center line. The two ground pads in injection GSSG pads are connected with the VCO ground. The two signal pads are floating. The signals on these pads are capacitively-coupled through the silicon substrate.

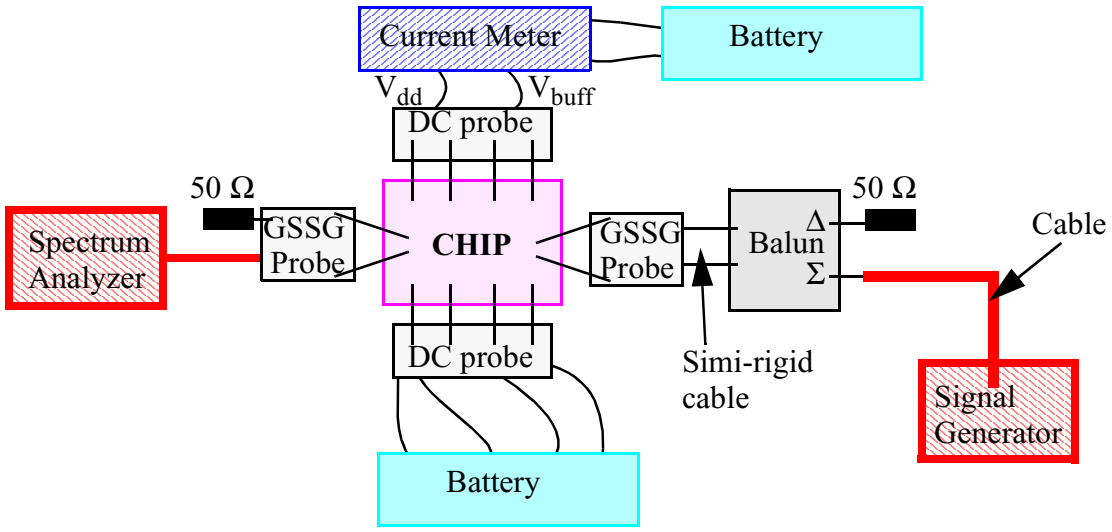


Figure 8-8 The VCO injection locking measurement setup

The VCO injection locking tests are performed on-wafer. The VCO output is landed with another GSSG probe. The measurement setup is illustrated in Figure 8-8. A signal generator provides an external injection signal, which is fed into a balun. The balun generates two signals with the same amplitude which is either in-phase (through Σ port) or 180^{o} out-of-phase (through Δ port). Thus, the VCO can be tested for the common mode and differential mode injection. The outputs of the VCO are captured using a spectrum analyzer. Batteries are used to provide all DC bias and supplies using DC probes.

8.3.3 Testing of the VCO Injection Locking

The VCO's have been measured for the locking bandwidth when the injection signal present. As mentioned there are three types of VCO's: VCO_standard, VCO_ind and VCO_subcont, and the on-chip bypass capacitors can be cut by a laser after the chip fabrication. Four different bypass configurations were examined: (1) with all the bypass capacitors shown in Figure 8-5; (2) without the bypass capacitor connected to V_{bias}, i.e., without C_{bp1}; (3) without the bypass capacitor connected to comm node, i.e., without C_{bp2}; (4) without the bypass capacitor connected to V_{tune}, i.e., without C_{bp3}. Thus, the total number

Table 8-4 Measured VCO locking bandwidth under the fundamental injection

VCO Type		with all bypass cap	without C_{bp1} (V_{bias})	without C_{bp2} (Comm)	without C_{bp3} (V_{tune})
Injection Type		Fundamental Injection (~5.8 GHz)			
Common Mode Injection	VCO_standard (MHz)	6.6	8.6	5.8	7
	VCO_ind (MHz)	1.9	1.7	3.1	3.9
	VCO_subcont (MHz)	7.2	9.5	6.6	9.8
Differen-tial Mode Injection	VCO_standard (MHz)	40.4	29.3	19.1	25.8
	VCO_ind (MHz)	8.6	7.5	9.7	8
	VCO_subcont (MHz)	45.6	30.5	24	29.4

Table 8-5 Measured VCO locking bandwidth under the 2nd superharmonic injection

VCO Type		with all bypass cap	without C_{bp1} (V_{bias})	without C_{bp2} (Comm)	without C_{bp3} (V_{tune})
Injection Type		2nd Superharmonic Injection (~11.6 GHz)			
Common Mode Injection	VCO_standard (MHz)	3.9	1.8	5.4	6
	VCO_ind (MHz)	0.9	0.1	3.3	3.7
	VCO_subcont (MHz)	6	2.8	7.5	11.7
Differen-tial Mode Injection	VCO_standard (MHz)	11.5	11.8	3.4	8.2
	VCO_ind (MHz)	4.7	3.6	0.7	3
	VCO_subcont (MHz)	15.4	15.9	6.1	18.6

of measured VCO structures is 3x4=12. These have been tested for both the common mode injection and differential mode injection. The bias conditions under the measurement for all VCO's are 1.5-V V_{dd} and 4-mA current.

For the fundamental injection, the injection signal is close to the VCO free running frequency which is around 5.8 GHz, and its power level is fixed. The measured VCO locking bandwidths under different situations are summarized in Table 8-4. The same locking

bandwidth testing is also used for the 2nd superharmonic injection study. The measurement results are listed in Table 8-5.

Several observations can be made based on these results:

1) For common mode injection, both common mode fundamental and 2nd superharmonic injection, there is not obvious difference between the locking bandwidth for VCO_standard and VCO_subcont. For the differential injection, VCO_subcont only shows slightly larger locking bandwidth than VCO_standard. These indicate that the p^+ guard ring does not provide significant advantage. In fact, it may have detrimental impact. The guard ring could give good isolation when the ground plane is perfectly grounded, the external signals may be more easily injected into the VCO through the guard ring when it is not perfectly grounded.
2) Though the testing is performed using the high frequency probes, the probe tips still have inductance which could cause the ground connections at 5.8 and 11.6 GHz to be less than perfect. An evidence to support this are the measurement data from the 2nd superharmonic common mode injection testing. Table 8-5 shows that for the VCO's without C_{bp1}, the locking bandwidths are the smallest. From the theoretical analysis, we know that the V_{bias} node is the most sensitive node for 2nd superharmonic injection. For the VCO's without C_{bp1}, the locking bandwidth should be the largest, but the measurement gives the opposite results. The explanation for this is that because the ground connection is imperfect, instead of grounding V_{bias} node, C_{bp1} provides a path for the injected signal to reach V_{bias} node. Thus VCO's without C_{bp1} shows the smallest locking bandwidth since the isolation between V_{bias} and the injection point is increased.

3) The fact that the circuit ground plane is not perfect is also supported by the measurement data from VCO_ind and VCO_standard. The inductor in VCO_ind is not shielded. The injected signal can coupled to the inductor through substrate resistance and inductor parasitic capacitance. VCO_standard has a fully-ground-shielded inductor, which is isolated from the substrate capacitive coupling, and should show a smaller locking range than the VCO_ind. But the measurement data are once again opposite, VCO_ind displays much a smaller locking bandwidth than the other two. Comparing VCO_ind and VCO_standard, the only difference is the ground shield for the inductor. These data also imply the most external signal has been injected through the inductor. This occurs when the ground plane is made to bounce by the external signal. The external signal is more easily spread by the ground plane and ground shield, and more easily coupled to the inductor through the large parasitic capacitor between the inductor and ground shield.
4) For the fundamental injection, comparing the common mode and differential mode injections, the differential injection show much larger locking bandwidth than the common mode injection. This matches the theoretical analysis results if the injection into the core transistor dominates. Since the most injection is through the inductor, the injection into the core transistor through the inductor will dominate. The gain for the fundamental differential injection into the core transistor is $a_1 A_i$, and for the common mode is $\sim 3/2 a_3 A_0 A_i^2$. The differential injection should have much large gain and large locking bandwidth.
5) For the 2nd superharmonic injection, comparing the common mode and differential mode injection, the differential injection also show a larger locking bandwidth than the

common mode injection. For the injection into core, the gain of the 2nd superharmonic common mode injection is ~$2a_2A_0A_i$, and the gain of the differential injection depends on the circuit symmetry. This testing indicates that even for a symmetric differential layout, the on-chip VCO circuit still has sufficient asymmetry, which causes injection locking. In particular cross coupling in VCO layouts cannot be perfectly symmetric.

6) For the differential mode injection, both fundamental injection and 2nd superharmonic display a small locking bandwidths for one situation: VCO's without C_{bp2}. Since C_{bp2} connects only the "comm" node in Figure 8-5, it is not clear why it affects the differential mode injection, while it has little effects on the common mode injection. More work is needed to understand this phenomena.

The injection locking tests are also performed for 1/2 subharmonic, 2/3 fractional and 3/2 fractional injection, however, no VCO can be injection locked with those types of injection.

As mentioned before, the two signal pads in the injection GSSG pad frame are floating and their parasitic capacitance is used to couple signals to the silicon substrate. When the injection signal frequency is changed, the incident power changes since the input impedance changes. In order to make the comparison among different types of the injection fair, the input voltage swings at the injection pads should be kept the same. To accomplish this, the injection pads input reflect coefficients have been measured over the frequency, and the input power is adjusted to keep a constant voltage amplitude. Under this condition, a second set of injection locking tests is carried out for VCO_standard with different bypass capacitors. The measurement results are summarized in Table 8-6. The input voltage amplitude is 0.86 V. Four types of injection locking have been tested: 1/2

Table 8-6 Measured VCO_standard locking bandwidth with the same input voltage

Injection Type		1/2 subharmonic	fundamental	2nd superharmonic	3rd superharmonic
Common Mode Injection	with all bypass cap (MHz)	Not Observed	8.5	6.6	2.3
	without C_{bp1} (V_{bias}) (MHz)	Not Observed	6.8	2.2	3.8
	without C_{bp2} (Comm) (MHz)	Not Observed	6	5.8	2.6
Differential Mode Injection	with all bypass cap (MHz)	Not Observed	41	15.5	4.4
	without C_{bp1} (V_{bias}) (MHz)	Not Observed	31	15	4
	without C_{bp2} (Comm) (MHz)	Not Observed	18.5	5.8	4.2

subharmonic, fundamental, 2nd superharmonic and 3rd superharmonic injection; and three different bypass capacitor configurations are examined: with all bypass capacitors, without C_{bp1} and without C_{bp2}.

From Table 8-6, some observation can drawn.

1) For the common mode injection, the fundamental and 2nd superharmonic injections show similar locking bandwidths, for VCO's with all bypass capacitors and without C_{bp2}. From the injection locking theoretical analysis, the 2nd superharmonic should have a large locking bandwidth than the fundamental injection. But for the injection into the core transistor, the fundamental injection also depends on the circuit symmetry. The comparable locking bandwidth of the fundamental injection indicates the symmetry of this differential VCO is not as good as expected.

2) For the differential mode injection, the fundamental injection shows a larger locking bandwidth than the 2nd superharmonic injection, which matches the theoretical analysis.
3) The 1/2 subharmonic injection is the hardest one to be locked. This is consistent with the theoretical analysis.
4) The 3rd superharmonic injection has a smaller locking bandwidth than the 2nd superharmonic injection for all cases.

Though the injection locking comparison among different types involves the coupling between the circuit and the injection point which are highly dependent on actual implementation, the measurements are still useful because they provide the experimental bases for the design approaches to mitigate injection locking. From the theoretical analyses and measured data, some guidelines for reducing VCO injection locking are listed.

1) Because of finite inductance between chip ground and board ground, the on-chip ground is always bouncing and not a perfect ground. The VCO circuit design has to include this as a design consideration.
2) When the working frequency is high such that the ground could cause the problems, do not use the shielded inductor or lower the ground inductance.The use of bypass capacitors should also be carefully considered. The bypass capacitors at V_{bias} node (C_{bp1}) and at comm node (C_{bp2}) as shown in Figure 8-5 are not suggested.
3) Avoid the differential mode injection. If possible, the power amplifier should be single-ended instead of differential. The physical distance between the power amplifier and VCO should be increased to reduce the coupling.

4) In the VCO frequency plan, avoid the fundamental and 2nd superharmonic injection. Even the 3rd superharmonic is not good. The subharmonic and fractional injection should be used.
5) Using a small inductor and an inductor with a high inductor quality factor to improve VCO phase stability, will increase the resistance to injection locking.

8.4 Summary

The VCO injection locking is an important design issue for a fully integrated transceiver, where the power amplifier and VCO are in the same chip. This work has utilized a commonly used differential LC VCO to study this phenomena. A theoretical analysis is given first. Based on it, injection locking VCO test circuits have been designed and fabricated. The test structures were characterized and the primary testing data were presented. Several observations are deducted from the theoretical analyses and the measurements. Finally, a set of design guidelines has been suggested.

CHAPTER 9
SUMMARY AND FUTURE WORK

9.1 Summary

A tunable multi-band radio frequency (RF) receiver for wireless LAN applications, and a feasibility study for the receiver are proposed in Chapter 2. The feasibility study has two major parts. First, the WLAN receiver implementation using CMOS technology has been a controversial topic. The skeptics agree on the advantages of CMOS for integration and low cost but doubt the CMOS RF circuit performance, especially at 5 – 6 GHz frequency range. With the wireless market dominated by SiGe transceivers when this work was started, there were uncertainties whether CMOS technology could achieve comparable performance. The demand for a multi-band function is increasing and the second part of the study has been evaluating whether the function could be realized in one-single RF block with a reduced area.

This feasibility study has been carried out at the RF block level, though the integrated receiver is the ultimate target. This reduces risks, since it is easier to obtain properly functionary RF blocks than an entire receiver. The list of key RF blocks includes RF switches, low noise amplifier (LAN), mixers and voltage controlled oscillators (VCO's).

Three RF CMOS switches working at 2.4, 5.8 and 15 GHz are designed and tested. The 2.4-GHz CMOS switch achieves adequate performance to meet the IEEE 802.11b specifications. The 5.8-GHz CMOS switch attained a comparable insertion loss as GaAs switches but with lower power handling capability. The investigation of methods to

increase the CMOS switch power handling capability has been continued by implementing two 15-GHz CMOS switches. By using integrated LC impedance transformation networks, the P_{1dB} of CMOS switch has been improved by 6.5 dB without sacrificing the switch insertion loss. The overall switch performance demonstrates that it is feasible to use CMOS switches instead of GaAs switches for many applications.

A wide tuning range voltage controlled oscillator (VCO) which is a key block (LO2) in the proposed multi-band receiver was presented in Chapter 5. The divider integrated with this VCO is also measured. The output frequencies cover the required 350 – 550 MHz range. The measured phase noise is only -114.5 dBc/Hz at 100 kHz offset. These are sufficient for wireless LAN applications. The demonstration of a wide tuning range VCO-divider combination with excellent phase noise is a significant step toward the realizing the proposed receiver.

With the wide tuning range VCO (LO2), the high frequency VCO required by the proposed multi-band receiver can operate at a fixed frequency, which can be used to achieve better phase noise. Such a multi-standard and multi-band VCO has been demonstrated with the lowest phase noise ever reported for CMOS VCO's in the four frequency bands it operates. The VCO supports four frequency bands (2.4, 2.5, 4.7 and 5.0 GHz) by using switched inductors and capacitors. With a 1-V power supply, the phase noise at 1-MHz offset is -126 dBc/Hz and -134 dBc/Hz in the 4.7 and 2.4 GHz bands. At 10-kHz offset, the phase noise is -75 dBc/Hz and -85 dBc/Hz in the 4.7 and 2.4 GHz bands, respectively. The VCO phase noise performance satisfies the WLAN requirement. With small adjustment in the frequency bands, it is suitable for the VCO1 in the proposed multi-band WLAN receiver.

A Low Noise Amplifier (LNA) is another key block for an RF receiver, which greatly affects the overall receiver noise figure thus sensitivity. CMOS technology has to prove that it can be used to implement low noise amplifiers operating in the 5 – 6 GHz range. To address this, a 5-GHz LNA is first implemented in a 0.18-μm CMOS process. With 2.16-dB noise figure, 16.2-dB power gain and 10 mW power consumption, it delivers not only sufficient but applaudable performance for wireless LAN applications. Encouraged by the 5-GHz LNA results, a double-band RF/IF down-converter was design and fabricated. By using switched resonators, band-selection and gain-switching functions are incorporated into a single circuit. The measured down-converter has adequate performance for wireless LAN applications. The successful demonstrations of a double-band RF/IF down-converter and a multi-band VCO illustrate that it is feasible to achieve tunable multi-band operation using a single RF block implemented in CMOS technology with reduced area and cost.

All key blocks, RF switches, wide-tuning range VCO, multi-band VCO and multi-band RF/IF down-converter, have been implemented and demonstrated. This demonstrate that it is feasible to achieve the proposed multi-band receiver by using CMOS technology.

In order to realize a fully integrated multi-band WLAN transceiver, the VCO injection locking has been theoretically and experimentally investigated. The VCO injection locking is the corruption of the VCO signal by an externally injected signal. This is critical for integration of a receiver and a transmitter. Both theoretically and experimentally, it is found that the 1/2 subharmonic injection is more resistant from being locked than the fun-

damental and 2nd Superharmonic injection. Based on the study, a set of design guideline to reduce the VCO injection locking is drawn.

9.2 Future Work

Based on the work presented in this thesis, a few future works are suggested.

9.2.1 Continuity of Injection Locking Testing

The VCO injection locking study included in this Ph. D. work provides a theoretical bases for understanding experimental observations. But, there are still many questions need to be answered. First, some testing results can not be explained. Second, based on the measurement results, the theoretical analyses need to include other effects to explain more real situations. For example, the ground inductance and transistor mismatch should be taken into account. Third, circuit simulations could be used to further support the explanations in Chapter 8. Fourth, VCO phase noise and power consumption should be measured with the injection locking bandwidth to explore the trade-offs. These will provide the guidelines for optimizing the VCO for the best overall performance for a chosen application. The last, this injection locking testing does not contain the study of a approaches to increase isolation between the circuit and injection point. This study is very important since increasing isolation directly reduces the locking bandwidth. In a nutshell, the injection locking is basic scientific study which can provide important insights for the circuit design, and should be continued.

9.2.2 Tri-Band WLAN Front-End

A dual-band RF/IF down-converter is demonstrated for 2.4 and 5.15 GHz band operation. The 5.725-5.825 GHz which is 802.11a high subband is not covered. The tradeoff of LNA gain and bandwidth can be specified by the LNA output tank Q [55]. If

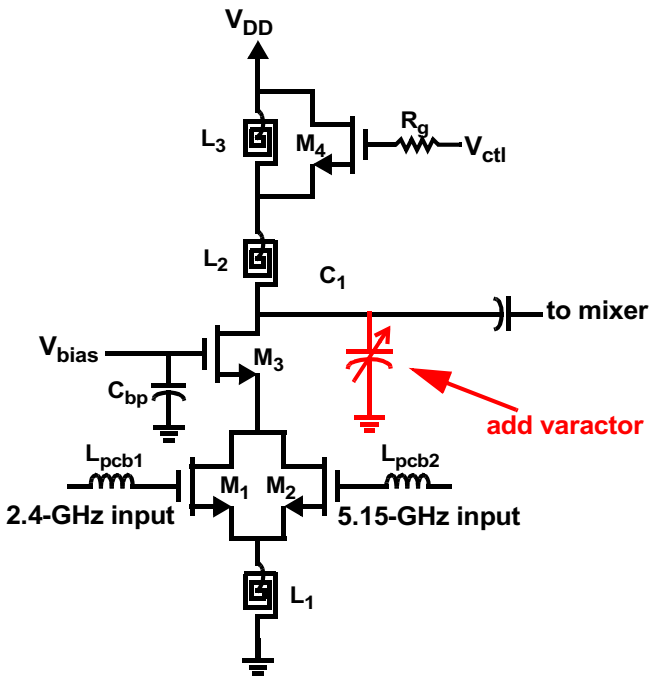


Figure 9-1 A schematic of tri-band low noise amplifier

the LNA has to cover from 5.15 to 5.825 GHz, the power consumption could be large due to low output tank Q. In contrast, a tunable circuit will have high gain with lower power consumption. One way to incorporate one more tunable band into the dual-band RF/IF down-converter is to place a varactor at the LNA output as shown in the Figure 9-1. A tri-band RF/IF down-converter can be realized with a switched resonator and a MOS varactor. Preliminary simulations indicate that a MOS varactor with the tunability of 2 and maximum capacitance of 200 fF could shift the output band between 5.25 and 5.8 GHz.

9.2.3 Integrated Multi-Band WLAN Receiver

The feasibility of multi-band WLAN CMOS receiver has been demonstrated by studying individual RF blocks. The integration of these blocks is another step toward the fully integrated transceiver. Integrating all blocks, such as switches, LNA, mixers and VCO's, into a single chip will most likely face new design challenges which may not be

overcome. But based on the feasibility study of individual blocks, a fully integrated CMOS multi-band WLAN receiver is possible.

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BIOGRAPHICAL SKETCH

Zhenbiao Li was born in Jingdezhen, Jiangxi province, People's Republic of China, in November, 1970. He received the Bachelor of Engineering in biochemical engineering with the highest honors from Shanghai Jiao Tong University, China, in 1992. In 2000, he received the Master of Engineering degree in electrical engineering from the University of Florida, Gainesville, Florida, USA. Since 1998, he has been working toward the Ph.D. degree at the SiMICS (Silicon Microwave Integrated Circuits and Systems) Research Group in the Department of Electrical and Computer Engineering at the University of Florida, Gainesville, Florida. Currently, he is a Ph.D degree candidate.

After his bachelor's degree, he worked in Shanghai Jiao Tong University as an associate in engineering until his studies in the USA. During the summer of 2000, he worked at Intersil Inc., Palm Bay, Florida, in the area of RFIC design, as a summer intern. From 2002 to 2003, he was with the Global Communication Devices, Inc., North Andover, Massachusetts, designing RF circuits for CMOS wireless LAN transceivers. For his Ph.D. dissertation research, he has been investigating the techniques to implement a multi-function and multi-band CMOS WLAN receiver system and circuits.